

IMPLEMENTATION OF NON-LINEAR CIRCUIT MODELS UNDER THE TLM

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Resume. We describe the inclusion of parametric behavioral macromodels within the Transmission-Line Modelling (TLM) method. The macromodels reproduce the input/output port non-linear behavior of digital integrated circuit (IC). They are generated with Mpilog software and integrated in the 3D electromagnetic code Minisolve. The numerical results are compared to experimental datas.

I. INTRODUCTION

On the Printed Circuit Boards (PCBs), the interconnection geometry influences the ElectroMagnetic Compatibility (EMC) and the Signal Integrity (SI). The impact increases when circuits with a non-linear behavior are connected at their terminations. An accurate EMC analysis requires an electromagnetic solver including the model of those non-linear components. The insertion is made via lumped elements within the mesh of the TLM code. This work follows the macromodel hybridization with the finite-difference time-domain (FDTD) method [1] example.

The paper is based on three parts. Sections II and III respectively recall the Mpilog software basis and TLM formulation used in Minisolve code. Section IV presents numerical and measurement results.

II. MPIOLOG

Mpilog (Macromodeling via Parametric Identification of Logic Gates) models the external port electrical characteristics of digital IC [2]. Relations (1) and (2) define the current of the input ports of receivers (1) -Fig. 1a)- and output ports of drivers (2) -Fig. 1b)-, in the discrete time and without considering the supply ports.

$$i_{\text{rec}}[k] = F_s(v[k]) + F_d(\Theta; v[k]) \quad (1)$$

$$i_{\text{drv}}[k] = w_H[k] \cdot i_H[k] + w_L[k] \cdot i_L[k] \quad (2)$$

where, k is the discrete time variable, $v[k]$ the voltage, $F_s(v[k])$ and $F_d(\Theta; v[k])$ the static and dynamic parts. A Local Linear State Space (LLSS) model (3) describes the dynamic component.

$$\begin{cases} x[k] & = A \cdot x[k-1] + B \cdot v[k-1] \\ F_d(\Theta; v[k]) & = C \cdot x[k] + D \cdot v[k] \end{cases} \quad (3)$$

w_H and w_L are switching signals accounting for the logic state evolution of the buffer. They are composed of concatenation of basic “up” and “down” signals computed during the model estimation process. i_H and i_L are similar to (1).

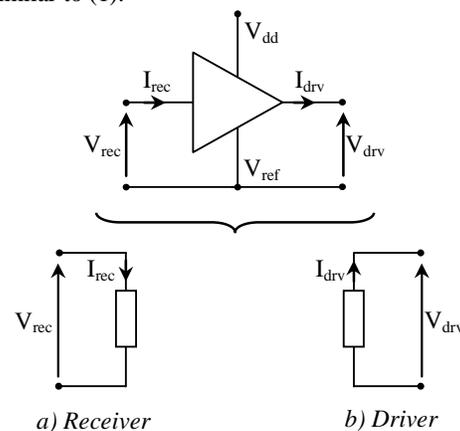


Fig. 1 – Input and output port models.
 V_{dd} and V_{ref} indicate the power supply voltages

Once the models created, they are readily embedded in any SPICE-like solvers or VHDL-AMS descriptions. Their datas are also available in a Matlab workspace. We use this file to retrieve all informations needed to the implementation of relations (1)-(3) in the TLM code.

III. TLM

This section deals with the implementation of the parametric models within the TLM. First of all it discusses the model inclusion. Then it presents the resampling procedure applied to the macromodels to match its sampling time to the one of the electromagnetic solver.

III.1. Minisolve

TLM is a differential time-domain method for solving field problems using circuit equivalent. The solution region is divided in elementary cells and the field components are calculated at the same location (cell center), at the same time.

Minisolve code [3] is based on the TLM formulation outlined in [4]. (4) gives a general expression of the voltage got at the center of a cubic node -see Fig. 2-, in Z domain, considering the z-oriented component.

$$V_z = T_e \left(2 \left\{ V_8^i + V_9^i + V_{10}^i + V_{11}^i \right\} - i_{fz} + z^{-1} S_{ez} \right) \quad (4)$$

where V^i denotes the incident voltages, $z^{-1} S_{ez}$ the previous event (6), i_{fz} the free electric current, T_e (5) and Γ_e (7) respectively the transmission and reflection coefficients of the node.

$$T_e = (4 + g_{e0} + 4\chi_{e0})^{-1} \quad (5)$$

$$S_{ez} = 2V_z^r + \Gamma_e V_z - \bar{g}_e(z)V_z + 4\bar{\chi}_e(z)V_z \quad (6)$$

$$\Gamma_e = -(4 + g_{e1} - 4\chi_{e1}) \quad (7)$$

$g_{e0}, g_{e1}, \bar{g}_e(z)$ and $\chi_{e0}, \chi_{e1}, \bar{\chi}_e(z)$ are the resulting components of the partial fraction expansion of the conductance and susceptibility ((23), (24) in [4]).

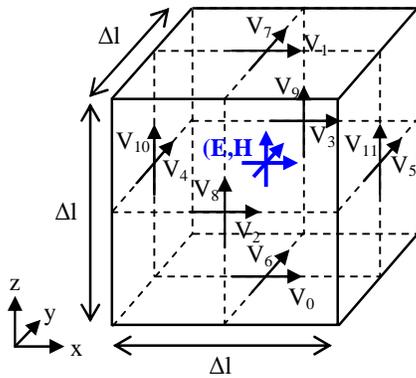


Fig. 2 – Three-dimensional TLM cell

Knowing the macromodel current-voltage relationship, we include the model via the conductance. We consider it as a black box in the mesh also no information is available on its previous state. The expressions (4)-(7) reduce thus in (9)-(12) for a z-oriented macromodel, considering the normalized conductance to the impedance of free-space η_0 (8).

$$g_{e0} = \eta_0 I_{\text{macro}} / V_{\text{macro}} \quad (8)$$

$$V_z = T_{e0} \left(2 \sum_{j=8}^{10} V_j^i + z^{-1} S_{ez} - \eta_0 I_{\text{macro}} \right) \quad (9)$$

$$T_{e0} = (4 + 4\chi_{e0})^{-1} \quad (10)$$

$$S_{ez} = 2V_z^r + \Gamma_{e0} V_z - \eta_0 I_{\text{macro}} \quad (11)$$

$$\Gamma_{e0} = -4 \quad (12)$$

Note that (9) and (11) are the relations for a receiver according to the sign conventions in Fig. 1. They are then modified by $+\eta_0 I_{\text{macro}}$ for a driver. In addition, (10) and (12) correspond to the coefficients of a free-space node. Hence the macromodel is inserted at the center of one free-space cell.

III.2. Resampling

The parametric model is established in the discrete time at the sampling time T_s . This time differs from the time step Δt of TLM code depending on mesh dimensions. The hybridisation implies a macromodel resampling from T_s to Δt . This is made by first converting the discrete-time model $x[k]$ (3) into a continuous-time model using the first-order forward approximation of the time derivative (13).

$$\frac{dx(t)}{dt} \Big|_{t=(k-1)T_s} \approx \frac{x[k] - x[k-1]}{T_s} \quad (13)$$

Then the system is resampled in the discrete-time to Δt (14)-(15).

$$\frac{dx(t)}{dt} = \frac{1}{T_s} \cdot \{[A - I]\} \cdot x(t) + B \cdot v(t) \quad (14)$$

$$x[k] = A_R \cdot x[k-1] + B_R \cdot v[k-1] \quad (15)$$

with

$$A_R = \left(I + \frac{\Delta t}{T_s} \cdot \{[A - I]\} \right) \quad B_R = \frac{\Delta t}{T_s} \cdot B \quad (16)$$

IV. VALIDATION

A PCB has been made to validate the hybridization. This section presents the measurements and the numerical results.

IV.1. PCB

Fig. 3 shows the test structure. It is made up of a driver (left side) and a receiver (right side) linked with a microstrip line. The strip is 800 μm wide, 100 mm long. The substrate has a 400 μm thickness, a relative permittivity $\epsilon_r = 4.24$ and dielectric losses of 0.01 at 1 MHz. In theory [5][6], this leads to a characteristic impedance $Z_c \approx 49.5 \Omega$ and an effective permittivity $\epsilon_{re} \approx 3.23$ (average at the frequencies of interest) either a propagation time $T_d \approx 0.6 \text{ ns}$ for $L = 100 \text{ mm}$. This length has been initially determined to perform simulations with the substrate height discretised in 3 cells. In that case L corresponds to the maximal length allowed by the PC resources. The current simulation is carried out with only 1 cell for the substrate height.

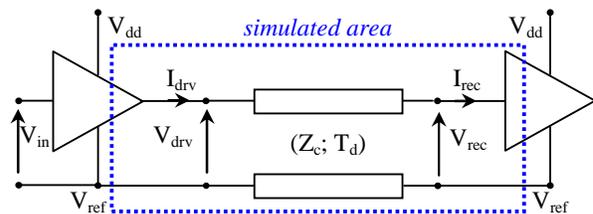


Fig. 3 – Test structure

The ICs are the SN74AHC1G04-Q1 single inverter from Texas Instruments (TI). They are supplied with ($V_{DD} = 4.8\text{ V}$; $V_{ref} = 0\text{ V}$).

The transient waveforms are collected with the LeCroy WavePro 7300A scope (3 GHz bandwidth, 10 GS/s) and the P6158 passive voltage probe (3 GHz bandwidth, 1 k Ω , 1.5 pF, 20x attenuation, 5ns delay). Fig. 5 reports the output (V_{drv}) and input (V_{rec}) port voltages got for the input voltage V_{in} : $V_M = V_{DD}$, $t_r = t_f = 10\text{ ns}$, delay = 13.9 ns, $W_{high} = 42.1\text{ ns}$, $T = 100\text{ ns}$.

IV.2. Macromodels

The receiver and driver macromodels are generated with the SN74AHC1GU04 HSPICE model, under the power supply: $V_{DD} = 4.8\text{ V}$; $V_{ref} = 0\text{ V}$. According to TI, this model applies to the SN74AHC1G04-Q1. The driver macromodel has a dynamic order of 3 and the receiver, 2. The models are established with the sampling time $T_s = 50\text{ ps}$.

IV.3. TLM structure

Fig. 4 shows the modelled structure in the TLM code. The dimensions are specified with the discretisation step $dl = 400\text{ }\mu\text{m}$, that corresponds to a time step $\Delta t = 0.67\text{ ps}$. The strip is zero-thickness and perfectly conducting, the substrate is assumed lossless. The configuration is surrounded by matched boundary conditions in the lateral and top directions and a perfect electric conductor one at the substrate back. The full-wave simulation carried out with a gaussian voltage source indicates a transmission line with $Z_c \approx 51\text{ }\Omega$ and $T_d \approx 0.67\text{ ns}$.

The strip is fed by the driver that the switching signals (2) are built from the measured voltage V_{in} . It is loaded by the receiver. The macromodels are implemented on one cell. Fig. 5 presents the full-wave simulation results as well as those of the HSPICE simulation. This last one is performed with the estimated macromodels and an ideal transmission line that the characteristics equal these ones of the full-wave simulation. A good agreement is observed. Note a difference at the transition end linked to the time delay of the probe (5 ns) that affects the signal measurements with fast switching time (around 3 ns here).

V. CONCLUSION

Models reproducing the I/O port non-linear behavior of IC have been implemented in a full-wave TLM solver. The comparison of numerical and experimental results have validated the hybridisation.

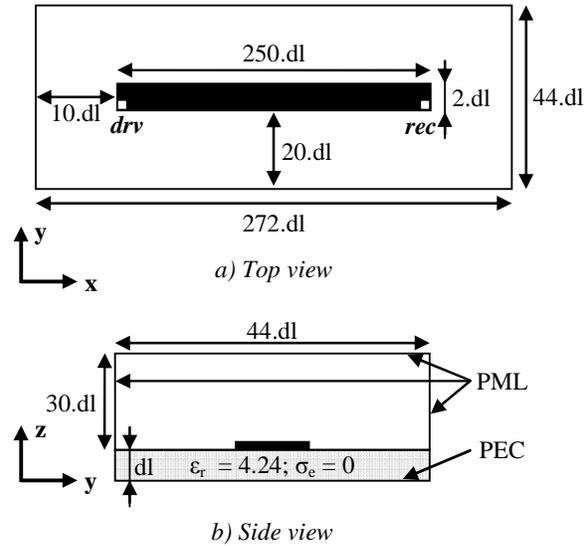


Fig. 4 – Microstrip structure used for validation

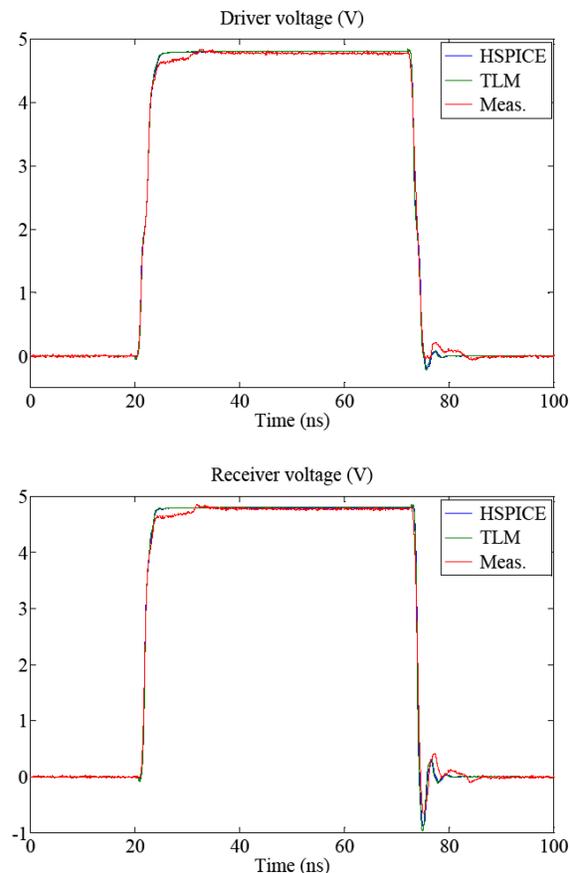


Fig. 5 – Comparison of driver (top) and receiver (bottom) voltages got by measurements and simulations with HPSICE and TLM

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