

# Control-Related Constraints, Optimization, and Scalability of Multi-Branch Multi-Level Flying Capacitor Converters (MBMLFCCs)

Category: Master Thesis  
Educational level: M.Sc. Electrical Engineering  
Research chair: Power Electronics and Electromagnetic Compatibility  
Start date: 10-Jan-2022

UT supervisor: Dr. Ir. Prasanth Venugopal  
Company supervisor: Dr. M.Sc. Jordi Everts

## Company

Prodrive Technologies is a developer and manufacturer of world-class electronics. It employs over 2100 people and is one of the fastest-growing companies in Europe. The organization is composed of two groups: Development and Operations. The Development department is oriented at developing high-end electronic, mechanic and software solutions. The operations department is responsible for production, assembly, testing and life-cycle management of electronic products and systems in the range of a few hundred to more than a million pieces per year.

## Context and application

Prodrive Technologies has developed a series of *amplifiers* that are used to drive inductive loads by generating large peak currents (>1000A) with a high change rate (>5000A/ms). The latter requires large amplifier output voltages of more than 2000V. Combined with the mentioned peak currents this leads to very high peak output power (>2MW) for the amplifiers.

The amplifiers that are investigated comprise multi-level, multi-branch (i.e., interleaved) *Flying Capacitor Converter (FCC) stages* that make use of the latest Silicon Carbide (SiC) semiconductor technology and are fed from a common high-voltage DC-bus. This facilitates a modular, low-volume, low-loss and low-cost design while offering the advantage of a high control bandwidth for the precise generation of the load currents due to an increased 'effective' switching frequency.

A range of amplifiers with varying power levels will be developed by taking advantage of the modularity and cost-effectiveness of this FCC based design. This drives the need for the derivation, simulation, and experimentation with *fundamental scaling laws* that link *control and output-quality constraints* (e.g., control bandwidth, output harmonics and ripple) to *hardware requirements* (e.g., number of branches and levels, output filter design), this derivation is the topic of this thesis.

## Assignment

The *main goal* of the thesis is to determine how control and output-quality requirements (e.g., control bandwidth, output harmonics and ripple) translate to hardware constraints (e.g., number of branches and levels, output filter design) that can be used in optimizing and scaling MBMLFCCs. This main goal is split up into four steps. As a *first step*, the relation between the control and output-quality requirements, and the hardware constraints imposed by these requirements will be investigated, leading to a design scope bound by the constraints. As a *second step*, the scalability of the MBMLFCC is investigated within this design scope by determining the optimal solutions (through component loss, lifetime, and cost models) for various output voltage- and current requirements using a to-be-defined non-black-box algorithm. Defining this algorithm is the *third step*. By combining the first three steps and varying the control and output-quality requirements as a *fourth step*, the direct effect of the requirements on the optimal hardware implementation can be investigated, ultimately leading to fundamental scaling laws for multi-branch multi-level FCCs.

## Focus Areas

The focus areas of the thesis comprise the four steps laid out above in more detail.

1. Investigation of how the control and output-quality requirements of the amplifier bound the hardware design space, leading to **control-related design-space constraints**. The methods and tools used are (1) open-loop frequency-domain analysis of the amplifier circuit and (2) stability analysis of the linearized dynamic system, both in MATLAB code. These models will be verified using measurements from a real multi-level multi-branch FCC amplifier.
2. Combining and expanding existing, separate, **component models** and adding those to the MATLAB-based frequency-domain model to calculate losses, cost, and lifetime of the amplifier. The goal is the derivation of **hardware-related design-space constraints** resulting in the operational space. The lifetime analysis also requires a thermal model and **load-profile** analysis, i.e., determining and simulating the 'worst' use-case.
3. Defining a non-black-box algorithm (e.g., iterative steps in a flow diagram) that can be applied to the combined frequency-domain and component models to find the **optimal solution** within the operational space (that is defined by the control and output-quality constraints, hardware constraints, and power requirements). As a verification, the optimal solution will be simulated in a closed-loop SIMULINK-PLECS model.
4. Investigation of the effect of the control and output-quality requirements on the optimal solutions by iterating on steps 1-3. Enabling the derivation of **fundamental scaling laws** for multi-branch multi-level FCCs that describe the relation between the requirements and the optimal solutions. This can be visualized as a superimposition of multiple optimal pareto regions for all the different requirements, giving an area constrained by all the requirements.