Generating *All* 2-Transistor Circuits Leads to New Wide-Band CMOS LNAs

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Aim

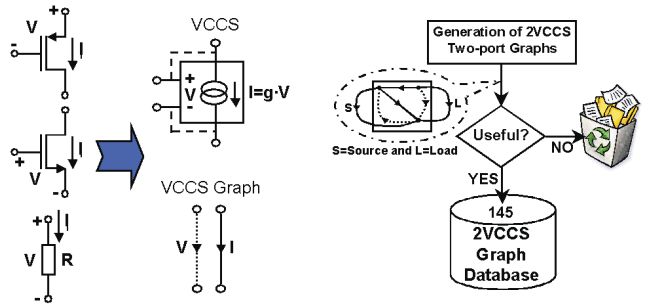
- Find *new* 2-Transistor wide band CMOS Low-Noise Amplifier (LNA) circuits.

Motivations

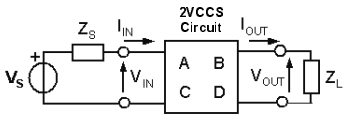
- Wide band LNAs are widely used in communication/instrumentation.
- *Few* different wide band LNAs alternatives in literature.
- Known LNAs are often simple circuits, which can be seen as 2-Transistor circuits or a combination of them.

Our Approach: Systematic Generation

- ***Systematic*** generation of ***ALL*** possible 2-Transistor circuits via graph based generation of ***ALL*** Two-ports with 2 VCCSs.

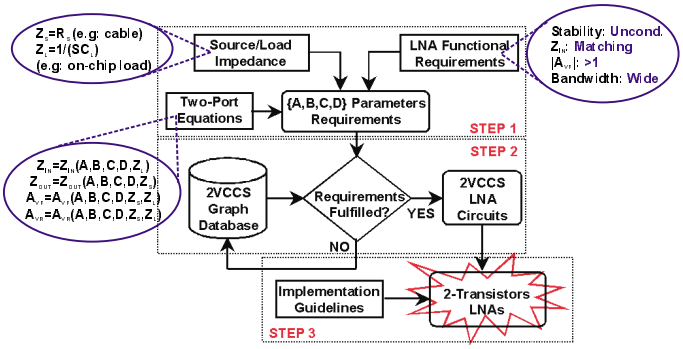


- 2VCCS Two-ports are characterized in terms of the *values and combinations* of {A, B, C, D} parameters, which depend on g_a and g_b (the transconductances of the 2 VCCSs), resulting in ***145 potentially usefull gaphs*** (the 2VCCS database) with at least ***one non-zero*** transmission parameter.



$A=V_{IN}/V_{OUT}$ for $I_{OUT}=0$ $\quad A=A(g_a,g_b)$
$B=V_{IN}/I_{OUT}$ for $V_{OUT}=0$ $\quad B=B(g_a,g_b)$
$C=I_{IN}/V_{OUT}$ for $I_{OUT}=0$ $\quad C=C(g_a,g_b)$
$D=I_{IN}/I_{OUT}$ for $V_{OUT}=0$ $\quad D=D(g_a,g_b)$

- **Generation of *ALL* 2-Transistor Wide Band LNAs:** within the 2VCCS database we find *ALL* the circuits that do behave as *wide band LNAs* using the following 3-steps methodology:



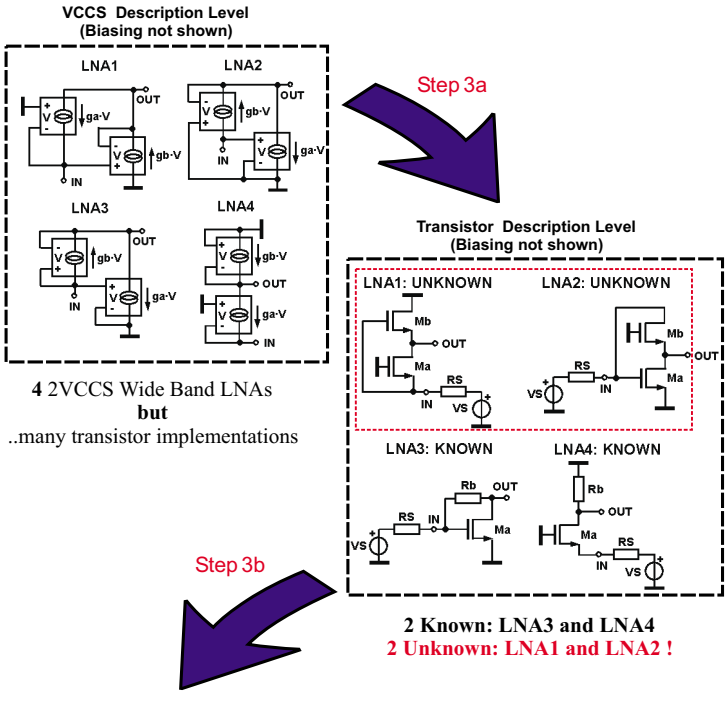
Step 1: LNA *small signal* functional requirements are translated into constraints for the {A, B, C, D} parameters upon proper source Z_S and load Z_L impedance (see the flow-chart).

Step 2: The 2VCCS graph database is explored for cases meeting the above requirements: ***these are 2VCCS Wide Band LNAs.***

Step 3: MOS transistor implementation:

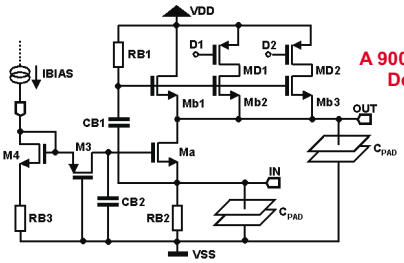
- a) VCCS: single NMOS (faster than PMOS) or Resistor (if possible).
- b) Circuit arrangement: *bias current re-use* is exploited to minimize DC power OR performance degradation due to biasing circuitry.

The Output of the Generation



4 2VCCS Wide Band LNAs
but
..many transistor implementations

2 Known: LNA3 and LNA4
2 Unknown: LNA1 and LNA2 !



A 900MHz Wide Band CMOS LNA Design Based on the LNA1

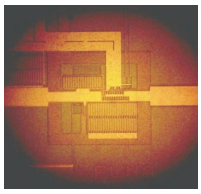
- Two-stages in Feed-forward: Mb1,2,3 *CS-stage* and Ma-Mb1,2,3 *CG-stage*.
- Input signal "ac" coupled to Mb1,2,3 via the CB1-RB1 high-pass filter.
- Variable Gain: from 6 to 12dB in 4 discrete steps.
- Switches out of the signal path ---> minimum performance degradation.

Measurements

A_{VF}	11dB
-3dB Bandwidth	900MHz
$VSWR_{IN}$	<1.6
A_{VR}	< -30dB
IIP2	15dBm
IIP3	1dBm
NF	< 4.5dB
Supply Voltage	3.3V
Supply Current	1.5mA
Technology	0.35µm CMOS
Die Area	0.06mm^2

Measurements at Max Gain: R_S=75Ω and C_L=0.2pF.

Chip Photo



Conclusions

- A methodology generating ***ALL*** 2-Transistors wide band LNAs has been presented, yielding to ***2 new*** circuits.
- An LNA prototype realized using an industrial 0.35µm CMOS process shows 900MHz bandwidth draining only 1.5mA, good linearity and NF<4.5dB (e.g.: suitable for cable modem or cable TV applications).
- This systematic generation approach can be used to select other class of linear circuits.

Acknowledgments

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