Test Review sessions in the

Module 5a
Creative Technology

Best practices and critical remarks

Erik Faber and Luuk Spreeuwers,
27th of October 2015
EWI Onderwijs Seminar

Acknowledgements

Smart Tech team

Cora Salm (EE)
Edwin Dertien (CreaTe/EE)
Mark Bentum (EE)
Geert Folkertsma (EE)
Gjerrit Meinsma (TW)
Peter Breedveld (EE)
Paolo Frasca (TW)
Joke Oosterhuis (OD)
Petri de Willigen (informatie specialist)
Erik Faber (CreaTe)

Context

Create offers specialisation (15EC) in module 5:

- Or New Media: audio, graphics, storytelling, game design, animated narration
- Or Smart Technology: technology behind “smart” products via 4 core topics:
  - Electric Circuits and Electronics
  - Sensors
  - Telecommunication
  - Control Systems

Module Design

15EC in 15EC module

Smart Tech Core: ~~15EC~~ 10.5EC

Math: ~~3EC~~ 2EC

Individual Project: 2EC

Tutoring: 0.5EC

TOM stimulates integration

- Find topics that fit together and form a theme
- Story line throughout the module
- Offer a subject when it is needed: e.g. complex numbers (math) at complex impedances (electric circuits)
- Test are progress tests of all topics at that moment → no longer “individual course” tests

Tests

- Theory (10.5EC) → 6 tests divided over 5 theory components (4x Smart Tech and 1x Math)

Tests

- Minimum grade per test: 5.0
- Every Monday morning a test
- With test in week x → resit in week x+2
- Conditions for participation in resit
  - Test (peer) review session (adapted from Luuk Spreeuwers - EE)

Example Schedule

14-15	Module 5a: Smart Tech				semester 1		Quartile 1		16 okt 2014 0:00		
	1	2	3	4	5	6	7	8	9	10	
	36	37	38	39	40	41	42	43	44	45	
	1 sep 2014	8 sep 2014	15 sep 2014	22 sep 2014	29 sep 2014	6 okt 2014	13 okt 2014	20 okt 2014	27 okt 2014	3 nov 2014	
			TESTS		TESTS	TESTS	TESTS	TESTS	Test Resit	RESIT	8:45
			Tst1(lg1): ac imp		Tst2(lg2):1,2orderEl	Tst3(lg3): sensors	Tst4(lg4): signals	Tst5(lg5): ModDynSy	Tst5(lg5): ModDynSy	Tst6(lg6,7): AnEl + C	10:30
	Kick off L: NM + ST	Project InfSpec L	Sys&Sign3 (2ndO)	Sys&sign5 (Sign f,t)	Project L	Control L	Project L	C&E11(d opamp)	Control7 L		10:45
	Project L: NM + ST	Project InfSpec L	Sys&Sign3 (2ndO)	Sys&sign5 (Sign f,t)	Project L	Control L	Project L	C&E11(d opamp)	Control7 L		12:30
Mo	C&E1 (Ohm)	C&E4 (C&L)	C&E7 (2nd step)	C&E9 (2nd Fil)	Project (self st)	Control T	Project (self st)	C&E 11 T	Control7 T		13:45 Mo
	C&E1 (Ohm)	C&E4 (C&L)	C&E7 (2nd step)	C&E9 (2nd Fil)	Project (self st)	Control T	Project (self st)	C&E 11 T	Control7 T		15:30
		C&E5 (1st step)	Sens3 L (Magn)		Project (self st)	Telecom5	Project (self st)				15:45
		C&E5 (1st step)	Sens3 L (Magn)		Project (self st)	Telecom5	Project (self st)				17:30
	2 sep 2014	9 sep 2014	16 sep 2014	23 sep 2014	30 sep 2014	7 okt 2014	14 okt 2014	21 okt 2014	28 okt 2014	4 nov 2014	
	Sensors1 L (Res)	Sens2 L (Cap)		Sys&Sign5 T / C&E	Sens5 L (ADDA)		Test Peer review	C&E10 T (diode.)	Lab Resit		8:45
	Sensors1 L (Res)	Sens2 L (Cap)		Sys&Sign5 T / C&E	Sens5 L (ADDA)		Tst3(lg3): sensors	C&E10 T (diode.)	Lab Resit		10:30
	C&E2 (superpos)	C&E T	Sys&Sign3 T / C&E	Telecom2	Telecom4	Sys&Sing6 (Lapl)	Sys&Sing7 (Lapl)	Test Peer review	Lab Resit		10:45
	C&E Tut	C&E T	Sys&Sign3 T / C&E	Telecom2	Telecom4	Sys&Sing6 (Lapl)	Sys&Sing7 (Lapl)	Tst4(lg4): signals	Lab Resit		12:30
Tue	Sens1 lab (6-9)	Sens2 Lab	Sens3 Lab	C&E / Telecom T	Sens5 Lab	Telecom Lab?		C&E Lab (Opamp)	Control 8 L		13:45 Tue
	Sens 1 lab (6-9)	Sens2 Lab	Sens3 Lab	C&E / Telecom T	Sens5 Lab	Telecom Lab?		C&E Lab (Opamp)	Control 8 L		15:30
	Vrijhof lab (6-9)	Sens2 Lab	Sens3 Lab		Sens5 Lab	Telecom Lab?	Control 4 L	C&E Lab (Opamp)	Control 8 T		15:45
	Vrijhof lab (6-9)	Sens2 Lab	Sens3 Lab		Sens5 Lab	Telecom Lab?	Control 4 L	C&E Lab (Opamp)	Control 8 T		17:30
	3 sep 2014	10 sep 2014	17 sep 2014	24 sep 2014	1 okt 2014	8 okt 2014	15 okt 2014	22 okt 2014	29 okt 2014	5 nov 2014	
	Sens1 lab (1-4)	Project guest L				Control2 L	Control 4 T	Control6 L	Project (self st)	Project presentation	8:45
	Sens1 lab (1-4)	Project guest L				Control2 L	Control 4 T	Control6 L	Project (self st)	Project presentation	10:30
	Vrijhof lab (1-4)	Sys&sign2 (CN)	Sys&sign4 (LTI)	C&E10 (diode,FET)	Telecom T	Control2 T	TESTS	Control6 T	Project (self st)	Project presentation	10:45
	Vrijhof lab (1-4)	Sys&sign2 (CN)	Sys&sign4 (LTI)	C&E10 (diode,FET)	Telecom T	Control2 T	Tst4, part 2: signals	Control6 T	Project (self st)	Project presentation	12:30
Wed	Tutoring (6-9)	Tutoring (6-9)	Tutoring (6-9)	Tutoring (6-9)	Tutoring (6-9)	Tutoring (6-9)	Tutoring (6-9)	Tutoring (6-9)	Tutoring (6-9)	Project presentation	13:45 Wed
	Tutoring (6-9)	Tutoring (6-9)	Tutoring (6-9)	Tutoring (6-9)	Tutoring (6-9)	Tutoring (6-9)	Tutoring (6-9)	Tutoring (6-9)	Tutoring (6-9)	Project presentation	15:30
	Vrijhof lab (6-9)	Project Self (6-9)	Project Self (6-9)	Project Self (6-9)	Project Self (6-9)	Project Self (6-9)	Project Self (6-9)	Project self (6-9)	Project self (6-9)	Project presentation	15:45
	Vrijhof lab (6-9)	Project Self (6-9)	Project Self (6-9)	Project Self (6-9)	Project Self (6-9)	Project Self (6-9)	Project Self (6-9)	Project self (6-9)	Project self (6-9)	Project presentation	17:30
	4 sep 2014	11 sep 2014	18 sep 2014	25 sep 2014	2 okt 2014	9 okt 2014	16 okt 2014	23 okt 2014	30 okt 2014	6 nov 2014	
		C&E6 (com imp)		Sens4 L (Acou)	Sens6 L (opt)	Telecom 6	Project (self st)	Control lab (PID)	Project (self st)		8:45
		C&E6 (com imp)		Sens4 L (Acou)	Sens6 L (opt)	Telecom 6	Project (self st)	Control lab (PID)	Project (self st)		10:30
	Sys&Sign1	Sys&Sign2 T / C&E	C&E8 (1st Fil)	Telecom3	Multiport&Matrix L	Telecom T	Project (self st)	Control lab (PID)	TESTS		10:45
	Sys&Sign1	Sys&Sign2 T / C&E	C&E8 (1st Fil)	Telecom3	Multiport&Matrix L	Telecom T	Project (self st)	Control lab (PID)	Tst6(lg6,7): AnEl + C		12:30
Thu	C&E3 (signals)	Self St. / GOGBOT	C&E Lab (2nd O)	Sens4 Lab	Sens6 Lab	Control3 L	Control5 L	Control lab (PID)	Project (self st)		13:45 Thu
	C&E3 (signals)	Self St. / GOGBOT	C&E Lab (2nd O)	Sens4 Lab	Sens6 Lab	Control3 L	Control5 L	Control lab (PID)	Project (self st)		15:30
	Telecom1	Self St. / GOGBOT	C&E Lab (2nd O)	Sens4 Lab	Sens6 Lab	Control3 T	Control5 T	Control lab (PID)	Project (self st)		15:45
	Telecom1	Self St. / GOGBOT	C&E Lab (2nd O)	Sens4 Lab	Sens6 Lab	Control3 T	Control5 T	Control lab (PID)	Project (self st)		17:30
	5 sep 2014	12 sep 2014	19 sep 2014	26 sep 2014	3 okt 2014	10 okt 2014	17 okt 2014	24 okt 2014	31 okt 2014	7 nov 2014	
		Self St. / GOGBOT	Test Peer review		Test Peer review			Test Peer review	Test Peer review	Final Resit	8:45
		Self St. / GOGBOT	Tst1(lg1): ac imp		Tst2(lg2):1,2orderEl			Tst5(lg5): ModDynSy	Tst6(lg6,7): AnEl + C	Final Resit	10:30
	Sys&Sign1 T /C&E	Self St. / GOGBOT	Sys&Sign4 T / C&E	C&E / Telecom T	Multiport& Matrix T	Sys&Sign6 T / Cont	Sys&Sign7 T / Cont			Final Resit	10:45
	Sys&Sign1 T /C&E	Self St. / GOGBOT	Sys&Sign4 T / C&E	C&E / Telecom T	Multiport& Matrix T	Sys&Sign6 T / Cont	Sys&Sign7 T / Cont			Final Resit	12:30
Fri	Project guest L	Self St. / GOGBOT	Project guest L	Test Resit		Test Resit	Test Resit	Test Resit			13:45 Fri
	Project guest L	Self St. / GOGBOT	Project guest L	Tst1(lg1): ac imp		Tst2(lg2):1,2orderEl	Tst3(lg3): sensors	Tst4(lg4): signals			15:30
		Self St. / GOGBOT									15:45
		Self St. / GOGBOT									17:30

Test Review sessions

- Test on a Monday → test review session same Friday

- Scheduled in the roster: every Friday morning 8.45 – 10.30

- Mandatory if insufficient mark on regular test
- Not mandatory if sufficient mark on regular test, bonus of 0.5point on regular test grade

Test Review sessions

- Review session: student discuss their test in groups of 4 – 5 (mix of sufficient and insufficient)

- Redo the question made insufficient

- Teacher checks results and decides allocation of bonus

Results

- Excellent peer learning environment on learning materials
- Evaluations: peer-reviews are experienced as helpful/useful
- Feedback during review sessions: students valued positive learning experience afterwards

Thank you for attention