# System Reliability with Formal Methods

**Introduction**
With the insistent increasing in the design complexity of integrated circuits, it is becoming apparent that full verification of large circuit designs can be a challenging task [1]. Verification is especially important in the context of space exploration, where hardware needs to be hardened for radiation harsh environments, and development cycles are expensive.

Recently, there is a move towards property driven hardware design methodologies and tools. However, the use of these methods for increasing the reliability of hardware against the effects of radiation is little explored.

**Expected outcome**

- Evaluation of literature with methods for increasing system reliability with formal methods.
- Setup of environment for Formal Verification [2].
- Formally evaluate a RISC-V processor using this setup.

**Requirements**

- Interest in embedded systems, dependable computing and/or formal methods.
- Programming experience in Python.
- Familiarity with HDL and FPGA design.

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**References**

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2. https://fvm.us.es/doc/main/index.html