Thesis Topic:

Resilient Scheduling through Performance Counter Monitoring on RISC-V under Soft-Errors

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Background:

Performance counters are specialized hardware registers that keep track of various aspects of software and hardware behaviors, such as cache misses, branch mispredictions, and instruction counts. These counters provide a granular view of an application's runtime behavior, making them invaluable for performance optimization and system analysis. Real-time scheduling, on the other hand, is crucial in systems that must adhere to strict timing constraints. As the cornerstone to realize such a system, real-time operating systems (RTOSes) like FreeRTOS prioritize tasks based on their time-sensitive requirements, ensuring that critical operations are executed within predetermined time limits.

Under the context of soft-errors, to mitigate the pessmistism induced by the static timing analysis, the state-of-the-art, such as [4], leverages the detection of soft-errors to decide when to execute the reliable but expensive execution versions. However, this system model does not precisely reflect the overhead of detection and recovery mechanisms, which is actually not negligible. The confluence of performance counters and real-time scheduling in an RTOS environment offers a promising avenue for this problem to avoid over-provision. Using performance counters to dynamically monitor the state and progress of tasks may provide an opportunity to make more efficient scheduling decisions. This adaptive approach could improve both the efficiency and reliability of real-time systems, thereby making this research significant in the evolving landscape of embedded and real-time computing.

Project Description:

This project aims to develop a real-time scheduling mechanism that takes into account the progress of an application based on performance counter monitoring. The student will develop a methodology to extract performance "checkpoints" from static code analysis, and then monitor them on a system executing the application.

The system itself is a RISC-V micro controller, with a proof-of-concept implementation of FreeRTOS. The student will then evaluate the impact of this monitoring in the scheduling, and the performance impact incurred by the method.

Key References:

1. Real time power estimation and thread scheduling via performance counters
2. Low-Overhead Online Assessment of Timely Progress as a System Commodity
3. Average Task Execution Time Minimization under (m, k) Soft Error Constraint

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Student Profile:

Skills Required:

- Proficiency in C programming

Desired Knowledge:

- Real-Time System
- Computer Architecture
- System Programming

Supervisor/Contact Information:

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How to Apply:

Send us an e-mail to k.h.chen@utwente.nl and b.endresforlin@utwente.nl, write a bit about your motivation to work on the subject, your background, and at what stage of the master program you are. We will then set a meeting.

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