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Electrical and structural characterization of PLD grown CeO_2–HfO_2 laminated high-k gate dielectrics

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Abstract

The electrical and physical properties of CeO_2–HfO_2 nanolaminates deposited by pulsed laser deposition (PLD) are investigated. The properties of the nanolaminates are compared with binary CeO_2 and HfO_2 thin films. Layers were deposited using CeO_2 and HfO_2 targets at substrate temperatures between 220 and 620 °C in 10 Pa $Ar+H_2$ or O_2. In situ post deposition anneal (PDA) was achieved by controlled cooling down to room temperature with $p_{O_2} = 10$ kPa. Nanolaminates starting with CeO_2 show lower EOT and leakage compared to layers starting with HfO_2. TEM and XRD analyses showed thickness-dependent crystallinity of the layers, varying from amorphous to highly oriented polycrystalline phase.

C–V and I–V measurements were done on the capacitors. Lowest fixed-charge density $Q_f = 4 \times 10^{12}\,cm^{-2}$ was found for the nanolaminates deposited at 520 °C. The k values of the nanolaminates extracted by the EOT-physical thickness plots were found to be 141, 48 and 22, for deposition temperatures 420, 520 and 620 °C, respectively. Higher k value for lower deposition temperatures is explained by the thickness dependent morphology of the layers. An EOT = 0.95 nm with $J_g = 1.1 \times 10^{-2}\,A/cm^2$ was found for binary HfO_2 layer with 4 nm physical thickness. Lowest leakage current density $J_g = 1.9 \times 10^{-7}\,A/cm^2$ was for a 4 nm laminate deposited at 420 °C and with a cooling rate of 2 °C/min during PDA.

Keywords: Pulsed laser deposition (PLD); Electrical

1. Introduction

The need for high-k gate dielectrics has been emphasized in numerous scientific reports [1,2]. The gate capacitance is one of the key factors for determining metal oxide semiconductor field effect transistor (MOSFET) performance [3]. The gate capacitance in scaled MOSFETs has to be kept high for a good control of the inversion charge by the gate voltage. For a high capacitance with smaller area, decreasing the dielectric thickness or increasing the dielectric constant is needed according to the parallel plate capacitor relation.

HfO_2 has received major attention as a high-k gate dielectric because of its moderate band gap (6 eV), high permittivity ($k = 25$), high thermal

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stability and good process compatibility [4]. Another promising candidate is cerium oxide. This material has two common stochiometries, CeO_2 and Ce_2O_3, with different thermodynamical stabilities on silicon (CeO_2: $\Delta G_{1000} = +36.290$ kcal/mol, Ce_2O_3: $\Delta G_{1000} = +104.946$ kcal/mol) and different electrical properties as well. Ce_2O_3 is one of the best thermodynamically stable materials on silicon. However, has a relative permittivity of $k = 7$, where CeO_2 has a $k = 26$ [4]. Another advantage of CeO_2, in fluorite structure, is its very low lattice mismatch (0.35%) with silicon, which is an advantage for epitaxial dielectrics for future applications. Its band gap of a 5.5 eV also meets the requirements for high-k dielectrics [5–7]. In this work, the electrical and physical properties of CeO_2–HfO_2 nanolaminates deposited by pulsed laser deposition (PLD) are investigated. The properties of the nanolaminates are compared with binary CeO_2 and HfO_2 thin films.

2. Experimental

Binary CeO_2 and HfO_2 layers and CeO_2/HfO_2 laminates are deposited by PLD on HF dipped silicon 001 substrates in 0.1 mbar Ar + (5%)H_2 and from CeO_2 and HfO_2 targets by using an energy density of 1 and 3 J/cm^2, respectively. Deposition is followed by an in situ oxidizing post deposition anneal (PDA) during cooling down from deposition temperature to room temperature with a cooling rate of 2 °C/min. First, the laminated structures consist of two different types of layer sequence, i.e. CeO_2–HfO_2–CeO_2–HfO_2 (C–H–C–H) and HfO_2–CeO_2–HfO_2–CeO_2 (H–C–H–C), with an individual layer thickness of 1 nm are deposited to investigate the effect of layer sequence. Additionally, C–H–C–H laminates with different thicknesses (from 2 to 16 nm) are deposited at various temperatures from 220 to 620 °C with the same PLD parameters, but with 5 °C/min cooling rate during PDA, for detailed analysis of the effect of deposition temperature on the properties.

The layers are characterized by X-ray photoelectron spectroscopy (XPS) and transmission electron microscope (TEM) analyses. Capacitance–voltage (C–V) and current–voltage (I–V) measurements are performed for electrical characterization of the layers.

3. Results and discussion

3.1. Structural characterization

Cross-sectional TEM images (Fig. 1) of the laminates deposited at 420 °C with two different layer sequences show the presence of crystallites in the H–C–H–C laminate, whereas the C–H–C–H laminate layer remains amorphous. This indicates that the Si–HfO_2 interface is more favorable for the formation of a crystalline phase. Additionally, a comparison of the TEM images of the laminates with CeO_2 binary oxide layer deposited at identical conditions (Fig. 2) reveals that the CeO_2 binary oxide layer, which has the Si–CeO_2 interface, also has crystallites. This shows that the crystalline phase formation is inhibited in case of the laminated structure in C–H–C–H layer sequence. Fast Fourier transformation (FFT) analysis on the TEM image of the H–C–H–C laminate revealed that crystallites formed in the layer are in tetragonal $CeHfO_4$ structure.

Another important aspect of the laminated layers that was obtained from TEM analyses is the dependency of their crystallinity on the layer thickness. As can be seen in Fig. 3, the laminated CeO_2–HfO_2 dielectric layer, with an estimated deposited thickness of 12 nm has a polycrystalline structure, whereas the 4 nm physical thickness layer shown in Fig. 1 is amorphous. This result can be

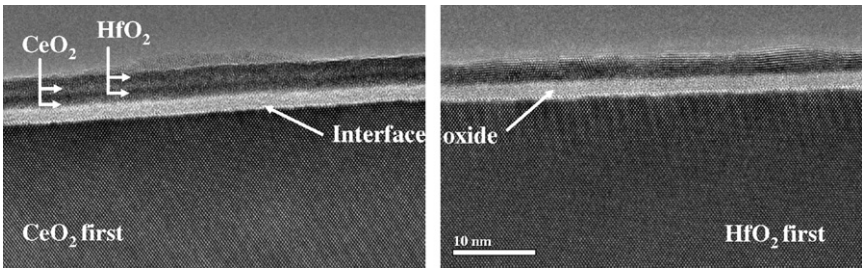

Fig. 1. TEM pictures of laminates with two different layer sequence. C–H–C–H (left), and H–C–H–C (right). Layers are deposited at 420 °C, in 10 Pa Ar + (5%)H_2 and had an in situ PDA at 10 kPa O_2.

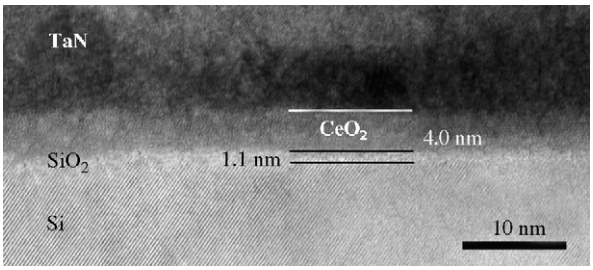

Fig. 2. Cross-sectional TEM pictures of CeO_2 layer deposited at identical conditions with the laminated layers shown in Fig. 1 (420 °C, 10 Pa Ar + (5%)H_2, followed by an in situ PDA at 10 kPa O_2).

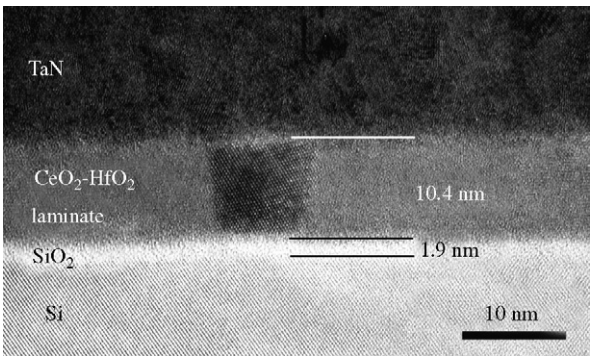

Fig. 3. Cross-sectional TEM picture of the CeO_2–HfO_2 laminated gate dielectric deposited at identical conditions with those presented in Fig. 1 (420 °C, 10 Pa Ar + (5%)H_2, followed by an in situ PDA at 10 kPa O_2), with an estimated deposited layer thickness of 12 nm.

explained by two different mechanisms: First, the time spent at high temperature, i.e. the deposition temperature (420 °C in this case), is longer in deposition of thicker layers than the thin layers and this might result in increased crystallinity in the layer. The second explanation for increased crystallinity in thicker layers is related to their volume-to-surface ratio: In case of thick layers this ratio is higher than the thin layers and this leads to higher crystallinity [8,9].

3.2. Electrical characterization

Electrical characterization of the layers is performed at room temperature on the MOS structures with different electrode areas (10^{-4}, 4×10^{-4} and $16\times10^{-4}\,cm^{-2}$) for monitoring the scaling of the leakage current density (J) and the capacitance by electrode area to prevent the measurement errors. C–V measurements are performed at three different frequencies, 10 kHz, 100 kHz and 1 MHz. Ten kHz data is used for determining the interface state density (D_{it}) by the method described by Carter et al. [10]. Hundred kHz and 1 MHz measurements are used for dual frequency series resistance correction [11]. Series resistance corrected capacitance is then processed by CVC simulation [12] for extracting the equivalent oxide thickness (EOT) and MOS device parameters as flatband voltage (V_{fb}). EOT extracted by CVC simulation is compared by the method uses a linear extrapolation of second derivative of capacitance in strong accumulation developed by Kar [13] for controlling purposes. Relative dielectric constants (k) of the layers are extracted from the slope of the plot of EOT versus deposited layer thickness (t_{ph}) of the layers. Fixed charge densities (Q_f) are calculated form the change of the V_{fb} of the layers by their thicknesses, from the slope of the V_{fb}–EOT plots.

The major difference between the laminates deposited at 420 °C in two different layer sequences, with a physical thickness of 4 nm, is found in their EOT and leakage current density values. These values are compared with those CeO_2 and HfO_2 binary oxide layers with the same physical thickness of 4 nm, which were deposited at identical conditions, and presented in Fig. 4. The HfO_2 layer has the lowest EOT of 0.95 nm, whereas the EOT of the C–H–C–H and H–C–H–C laminates are 2 and 2.6 nm, respectively. Low EOT of the HfO_2 binary layer than the other layers can be correlated to its higher crystallinity, hence higher k value, based on the fact that the Si–HfO_2 interface promotes crystallinity of the layers as shown in Fig. 1. The

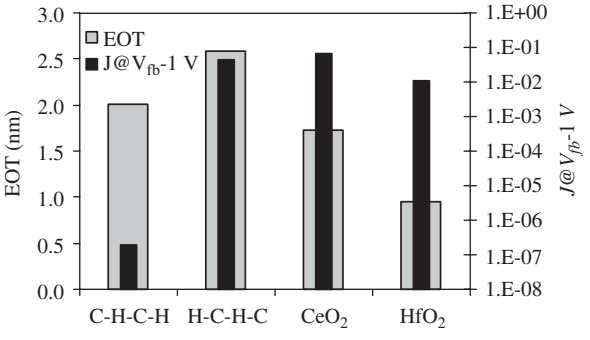

Fig. 4. EOT and leakage current densities (J at 1 V further than V_{fb} in accumulation) of the laminates deposited at 420 °C in two different layer sequences (as shown in Fig. 1) compared to CeO_2 and HfO_2 binary layers and deposited at identical conditions with the laminated dielectrics. All layers are in 4 nm physical thickness.

k value of the interface oxide, which affects the EOT of the stack, can also vary depending on its composition.

C–H–C–H laminate showed the lowest J at $V_{fb}-1$ V $= 1.88 \times 10^{-7}$ A/cm^2, which is about five orders of magnitude lower than the other layers. This large difference in the J of the layers is mainly correlated to the different structure of the layers: The C–H–C–H laminate was the only totally amorphous layer, whereas the other layers have polycrystalline structures, which the grain boundaries increases the leakage current density. However, one should also note the possible differences in the interface oxide, i.e. different starting layers may lead differences in interface oxide composition, and its effect on the EOT and J_g characteristics.

In order to understand the properties of the C–H–C–H sequenced laminates, a series of layers from 2 to 16 nm physical thicknesses were deposited at 420, 520 and 620 °C. MOS structures are prepared by TaN (for the layers deposited at 420 and 520 °C) and Au (for the layers deposited at 620 °C) electrodes. k values extracted from EOT vs. deposited layer thickness plots of the layers deposited at 420, 520 and 620 °C are found to be 141, 48 and 23, respectively. The extreme k value of the layers deposited at 420 °C is explained by the increased crystallinity of the layers with increasing thickness, which results in lower EOT for the thicker layers compared to those thinner and amorphous. This decreases the slope of the linear fit EOT–t_{ph} data hence yields to an unrealistic k value.

The Q_f of the laminated layers from the V_{fb}–EOT plots are found in the order of 10^{12} cm^{-2} for 420 and 520 °C deposition temperatures, whereas the binary CeO_2 layers have a Q_f in order of 10^{11} cm^{-2} for 520 °C deposition temperature. D_{it} of the laminates in order of 10^{11} eV^{-1} cm^{-2}, are in god agreement with binary CeO_2 layers and lower than binary HfO_2 layers with a D_{it} of 10^{12} eV^{-1} cm^{-2} levels.

4. Conclusions

The effect of the layer sequence in CeO_2–HfO_2 laminated dielectrics on the structural and electrical properties is presented. The Si–HfO_2 interface is found to improve the crystallinity of the layers compared to the Si–CeO_2 interface. It is also shown that the laminated structure diminishes the crystalline phase formation in the layers with a Si–CeO_2 interface. Four nm binary HfO_2 deposited at 420 °C has the lowest EOT of 0.95 nm. The only totally amorphous layer was the C–H–C–H laminate with an EOT of 2 nm, showed the lowest J at $V_{fb}-1$ V $= 1.88 \times 10^{-7}$ A/cm^2. The crystallinity of the laminates is found to be depending on their thicknesses and increasing with the increased layer thickness.

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