Electrical and structural characterization of PLD grown CeO$_2$–HfO$_2$ laminated high-$k$ gate dielectrics

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Abstract

The electrical and physical properties of CeO$_2$–HfO$_2$ nanolaminates deposited by pulsed laser deposition (PLD) are investigated. The properties of the nanolaminates are compared with binary CeO$_2$ and HfO$_2$ thin films. Layers were deposited using CeO$_2$ and HfO$_2$ targets at substrate temperatures between 220 and 620 $^\circ$C in 10 Pa Ar+H$_2$ or O$_2$. In situ post deposition anneal (PDA) was achieved by controlled cooling down to room temperature with $p$O$_2$ = 10 kPa. Nanolaminates starting with CeO$_2$ show lower EOT and leakage compared to layers starting with HfO$_2$. TEM and XRD analyses showed thickness-dependent crystallinity of the layers, varying from amorphous to highly oriented polycrystalline phase.

$C$–$V$ and $I$–$V$ measurements were done on the capacitors. Lowest fixed-charge density $Q_f = 4 \times 10^{12}$ cm$^{-2}$ was found for the nanolaminates deposited at 520 $^\circ$C. The $k$ values of the nanolaminates extracted by the EOT-physical thickness plots were found to be 141, 48 and 22, for deposition temperatures 420, 520 and 620 $^\circ$C, respectively. Higher $k$ value for lower deposition temperatures is explained by the thickness dependent morphology of the layers. An EOT = 0.95 nm with $J_g = 1.1 \times 10^{-2}$ A/cm$^2$ was found for binary HfO$_2$ layer with 4 nm physical thickness. Lowest leakage current density $J_g = 1.9 \times 10^{-7}$ A/cm$^2$ was for a 4 nm laminate deposited at 420 $^\circ$C and with a cooling rate of 2 $^\circ$C/min during PDA.

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1. Introduction

The need for high-$k$ gate dielectrics has been emphasized in numerous scientific reports [1,2]. The gate capacitance is one of the key factors for determining metal oxide semiconductor field effect transistor (MOSFET) performance [3]. The gate capacitance in scaled MOSFETs has to be kept high for a good control of the inversion charge by the gate voltage. For a high capacitance with smaller area, decreasing the dielectric thickness or increasing the dielectric constant is needed according to the parallel plate capacitor relation.

HfO$_2$ has received major attention as a high-$k$ gate dielectric because of its moderate band gap (6 eV), high permittivity ($k = 25$), high thermal
stability and good process compatibility [4]. Another promising candidate is cerium oxide. This material has two common stochiometries, CeO2 and Ce2O3, with different thermodynamical stabilities on silicon (CeO2: $\Delta G_{1000} = +36.290$ kcal/mol, Ce2O3: $\Delta G_{1000} = +104.946$ kcal/mol) and different electrical properties as well. Ce2O3 is one of the best thermodynamically stable materials on silicon. However, it has a relative permittivity of $k = 7$, where CeO2 has a $k = 26$ [4]. Another advantage of CeO2, in fluorite structure, is its very low lattice mismatch (0.35%) with silicon, which is an advantage for epitaxial dielectrics for future applications. Its band gap of a 5.5 eV also meets the requirements for high-$k$ dielectrics [5–7]. In this work, the electrical and physical properties of CeO2–HfO2 nanolaminates deposited by pulsed laser deposition (PLD) are investigated. The properties of the nanolaminates are compared with binary CeO2 and HfO2 thin films.

2. Experimental

Binary CeO2 and HfO2 layers and CeO2/HfO2 laminates are deposited by PLD on HF dipped silicon 001 substrates in 0.1 mbar Ar+(5%)H2 and from CeO2 and HfO2 targets by using an energy density of 1 and 3 J/cm2, respectively. Deposition is followed by an in situ oxidizing post deposition anneal (PDA) during cooling down from deposition temperature to room temperature with a cooling rate of 2°C/min. First, the laminated structures consist of two different types of layer sequence, i.e. CeO2–HfO2–CeO2–HfO2 (C–H–C–H) and HfO2–CeO2–HfO2–CeO2 (H–C–H–C), with an individual layer thickness of 1 nm are deposited to investigate the effect of layer sequence. Additionally, C–H–C–H laminates with different thicknesses (from 2 to 16 nm) are deposited at various temperatures from 220 to 620°C with the same PLD parameters, but with 5°C/min cooling rate during PDA, for detailed analysis of the effect of deposition temperature on the properties.

The layers are characterized by X-ray photoelectron spectroscopy (XPS) and transmission electron microscope (TEM) analyses. Capacitance–voltage (C–V) and current–voltage (I–V) measurements are performed for electrical characterization of the layers.

3. Results and discussion

3.1. Structural characterization

Cross-sectional TEM images (Fig. 1) of the laminates deposited at 420°C with two different layer sequences show the presence of crystallites in the H–C–H–C laminate, whereas the C–H–C–H laminate layer remains amorphous. This indicates that the Si–HfO2 interface is more favorable for the formation of a crystalline phase. Additionally, a comparison of the TEM images of the laminates with CeO2 binary oxide layer deposited at identical conditions (Fig. 2) reveals that the CeO2 binary oxide layer, which has the Si–CeO2 interface, also has crystallites. This shows that the crystalline phase formation is inhibited in case of the laminated structure in C–H–C–H layer sequence. Fast Fourier transformation (FFT) analysis on the TEM image of the H–C–H–C laminate revealed that crystallites formed in the layer are in tetragonal CeHfO4 structure.

Another important aspect of the laminated layers that was obtained from TEM analyses is the dependency of their crystallinity on the layer thickness. As can be seen in Fig. 3, the laminated CeO2–HfO2 dielectric layer, with an estimated deposited thickness of 12 nm has a polycrystalline structure, whereas the 4 nm physical thickness layer shown in Fig. 1 is amorphous. This result can be
explained by two different mechanisms: First, the time spent at high temperature, i.e. the deposition temperature (420°C in this case), is longer in deposition of thicker layers than the thin layers and this might result in increased crystallinity in the layer. The second explanation for increased crystallinity in thicker layers is related to their volume-to-surface ratio: In case of thick layers this ratio is higher than the thin layers and this leads to higher crystallinity [8,9].

3.2. Electrical characterization

Electrical characterization of the layers is performed at room temperature on the MOS structures with different electrode areas (10 × 10⁻⁴, 4 × 10⁻⁴ and 16 × 10⁻⁴ cm⁻²) for monitoring the scaling of the leakage current density (J) and the capacitance by electrode area to prevent the measurement errors. C–V measurements are performed at three different frequencies, 10 kHz, 100 kHz and 1 MHz. Ten kHz data is used for determining the interface state density (Dₓ) by the method described by Carter et al. [10]. Hundred kHz and 1 MHz measurements are used for dual frequency series resistance correction [11]. Series resistance corrected capacitance is then processed by CVC simulation [12] for extracting the equivalent oxide thickness (EOT) and MOS device parameters as flatband voltage (V₉f). EOT extracted by CVC simulation is compared by the method uses a linear extrapolation of second derivative of capacitance in strong accumulation developed by Kar [13] for controlling purposes. Relative dielectric constants (k) of the layers are extracted from the slope of the plot of EOT versus deposited layer thickness (tₚh) of the layers. Fixed charge densities (Q_f) are calculated from the change of the V₉f of the layers by their thicknesses, from the slope of the V₉f–EOT plots.

The major difference between the laminates deposited at 420°C in two different layer sequences, with a physical thickness of 4 nm, is found in their EOT and leakage current density values. These values are compared with those CeO₂ and HfO₂ binary oxide layers with the same physical thickness of 4 nm, which were deposited at identical conditions, and presented in Fig. 4. The HfO₂ layer has the lowest EOT of 0.95 nm, whereas the EOT of the C–H–C–H and H–C–H–C laminates are 2 and 2.6 nm, respectively. Low EOT of the HfO₂ binary layer than the other layers can be correlated to its higher crystallinity, hence higher k value, based on the fact that the Si–HfO₂ interface promotes crystallinity of the layers as shown in Fig. 1. The
The effect of the layer sequence in CeO$_2$–HfO$_2$ laminated dielectrics on the structural and electrical properties is presented. The Si–HfO$_2$ interface is found to improve the crystallinity of the layers compared to the Si–CeO$_2$ interface. It is also shown that the laminated structure diminishes the crystalline phase formation in the layers with a Si–CeO$_2$ interface. Four nm binary HfO$_2$ deposited at 420 °C has the lowest EOT of 0.95 nm. The only totally amorphous layer was the C–H–C–H laminate with an EOT of 2 nm, showed the lowest $J$ at $V_{fb}$ = 1.88 × $10^{-7}$ A/cm$^2$. The crystallinity of the laminates is found to be depending on their thicknesses and increasing with the increased layer thickness.

4. Conclusions

The effect of the layer sequence in CeO$_2$–HfO$_2$ laminated dielectrics on the structural and electrical properties is presented. The Si–HfO$_2$ interface is found to improve the crystallinity of the layers compared to the Si–CeO$_2$ interface. It is also shown that the laminated structure diminishes the crystalline phase formation in the layers with a Si–CeO$_2$ interface. Four nm binary HfO$_2$ deposited at 420 °C has the lowest EOT of 0.95 nm. The only totally amorphous layer was the C–H–C–H laminate with an EOT of 2 nm, showed the lowest $J$ at $V_{fb}$ = 1.88 × $10^{-7}$ A/cm$^2$. The crystallinity of the laminates is found to be depending on their thicknesses and increasing with the increased layer thickness.

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