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Characterization of Laminated CeO_2–HfO_2 High-*k* Gate Dielectrics Grown by Pulsed Laser Deposition

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The electrical and physical properties of CeO_2–HfO_2 nanolaminates on Si(100), by pulsed laser deposition, are investigated. Layers were deposited using pure CeO_2 and HfO_2 targets at various substrate temperatures ranging from 220 to 620°C at Ar + H_2 and O_2 and in situ postdeposition anneal of nanolaminates performed by controlled cooling from deposition temperature to room temperature under high oxygen pressure. After layer growth and anneal, top and bottom Au electrodes were deposited by sputtering. Electrical characterization was done by *C-V* and *I-V* measurements. The highest *k* value of 30 was found for the laminates deposited at 520°C in Ar + H_2 ambient. It is found that the properties of CeO_2–HfO_2 nanolaminates deposited at reducing atmosphere are dependent on the layer thickness. Thicker layers showed a higher dielectric constant and higher leakage current densities than thinner layers.
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As a result of aggressive scaling of the dimensions of complementary metal-oxide silicon (CMOS) devices, research on new high dielectric constant (high-*k*) materials for replacing SiO_2 has become a major issue in materials science of dielectrics in recent years. HfO_2 is the most promising candidate, and has been investigated intensively by the semiconductor industry and research institutions. CeO_2 is also one of the promising candidates because it is thermodynamically stable on silicon, which is advantageous for reducing interfacial SiO_2 regrowth.[1] CeO_2 with its fluorite structure has a very small lattice mismatch of 0.35% on silicon that allows epitaxial or highly oriented crystalline layers. CeO_2 also has a *k* value of 20–26 and a bandgap of approximately 6 eV.[2]

Laminated structures are used for tailoring the electrical and physical properties of oxides.[3] Conduction and valence band offsets the dielectric constant and in particular the leakage current properties of the resulting composite dielectric can be engineered by lamination. Pulsed laser deposition (PLD) is known for its flexibility and precision for growing atomically smooth alternating layers on various substrates.[4] In this work, first results of laminated CeO_2–HfO_2 dielectric layers deposited by PLD are presented.

Experimental

CeO_2–HfO_2 nanolaminates were grown on HF-dipped silicon (100) substrates at temperatures varying from 220 to 620°C by PLD from high-density, pure (above 99.99% purity) CeO_2 and HfO_2 targets in an ultrahigh vacuum (UHV)-PLD system (with a base pressure below 5×10^{-9} mbar). A 248 nm KrF laser is used for PLD at 1 and 3 J/cm^2 for CeO_2 and HfO_2 targets, respectively. Target-to-substrate distance was 45 mm and laser repetition rate was 5 Hz for all deposited layers. These settings resulted in a deposition rate of 0.125 nm/s. A 0.1 mbar Ar + H_2 (5%) gas mixture was used as deposition ambient to create a reducing atmosphere to prevent excessive silicon oxide formation during deposition, as well as to reduce the CeO_2 first layer to Ce_2O_3. The latter is thermodynamically more stable on silicon than CeO_2 toward SiO_2 growth. The Gibbs free-energy changes at 1000 K (ΔG_{1000}) for the SiO_2 formation reactions in contact with silicon are +36.3 and +104.9 kcal/mol for CeO_2 and Ce_2O_3, respectively.[1]

In situ postdeposition annealing (PDA) at high oxygen pressure from deposition temperature to room temperature with a controlled cooling rate (5°C/min) is used to oxidize the layers after deposition. To study the effect of the reducing deposition ambient, another series of layers was deposited using O_2 instead of Ar + H_2 gas mixture, at the same gas pressure of 0.1 mbar, in order to keep the kinetic energy of the ablated species the same. Each laminated structure consists of approximately 1 nm physical thickness alternating layers of CeO_2 and HfO_2, and CeO_2 is always used as the starting layer.

After deposition of the laminates, Au electrodes are deposited by sputtering via a shadow mask. The back sides of the substrates are also coated with a thin Au layer to create an ohmic contact and to decrease the series resistance during electrical measurements.

Results and Discussion

Growth of CeO_2–HfO_2 nanolaminates.— Figure 1 shows atomic force microscope (AFM) images of laminated CeO_2–HfO_2 layers deposited by PLD at various deposition temperatures from 220 to 520°C. The layers were deposited in a reducing deposition atmosphere followed by the in situ PDA. The layers have comparable roughness with the substrates, even at 220°C deposition temperature, where surface mobility is limited compared to the ones deposited at higher temperatures.

According to X-ray photoelectron spectroscopy (XPS) measurements, PDA establishes a complete oxidation of layers but also results in thicker interfacial oxides compared to those without in situ PDA. Interface thickness measurements based on XPS spectra of Si 2p peaks showed that the interfacial oxide thickness also depends on the deposition temperature (Fig. 2).

The observed interface layer (IL) thickness by transmission electron microscope (TEM) pictures is smaller than that measured by XPS analysis, which might be a result of SiO_2 diffusion into the first layer of the laminate. This can be seen in Fig. 3a and Fig. 3b, where TEM cross section images of two layers deposited at 420 and 520°C are shown, respectively. An amorphous laminated structure is clearly visible in the layer deposited at 420°C, whereas crystallization is observed in the layer deposited at 520°C. Although the individual layers are hardly discerned in the latter, it is still present. TEM and X-ray diffraction (XRD) analyses also showed that CeO_2–HfO_2 laminates tend to form tetragonal $CeHfO_4$ structure at elevated temperatures. However, note that the crystals are compatible with cubic (fluorite) CeO_2 and HfO_2 structures. The (101) texture of $CeHfO_4$ is equivalent to the (111) CeO_2 cubic structure. The possible transformation from cubic CeO_2 to tetragonal $CeHfO_4$ is not likely to involve complete recrystallization of the layer, but merely a deformation of the CeO_2 lattice when HfO_2 diffuses in due to this large similarity. Interface thicknesses of layers are 1.6 nm for 420°C and 1.9 nm for 520°C, less than what was found by XPS analyses.

Electrical measurements.— Capacitance-voltage (*C-V*) measurements of laminated structures are difficult to interpret, particularly

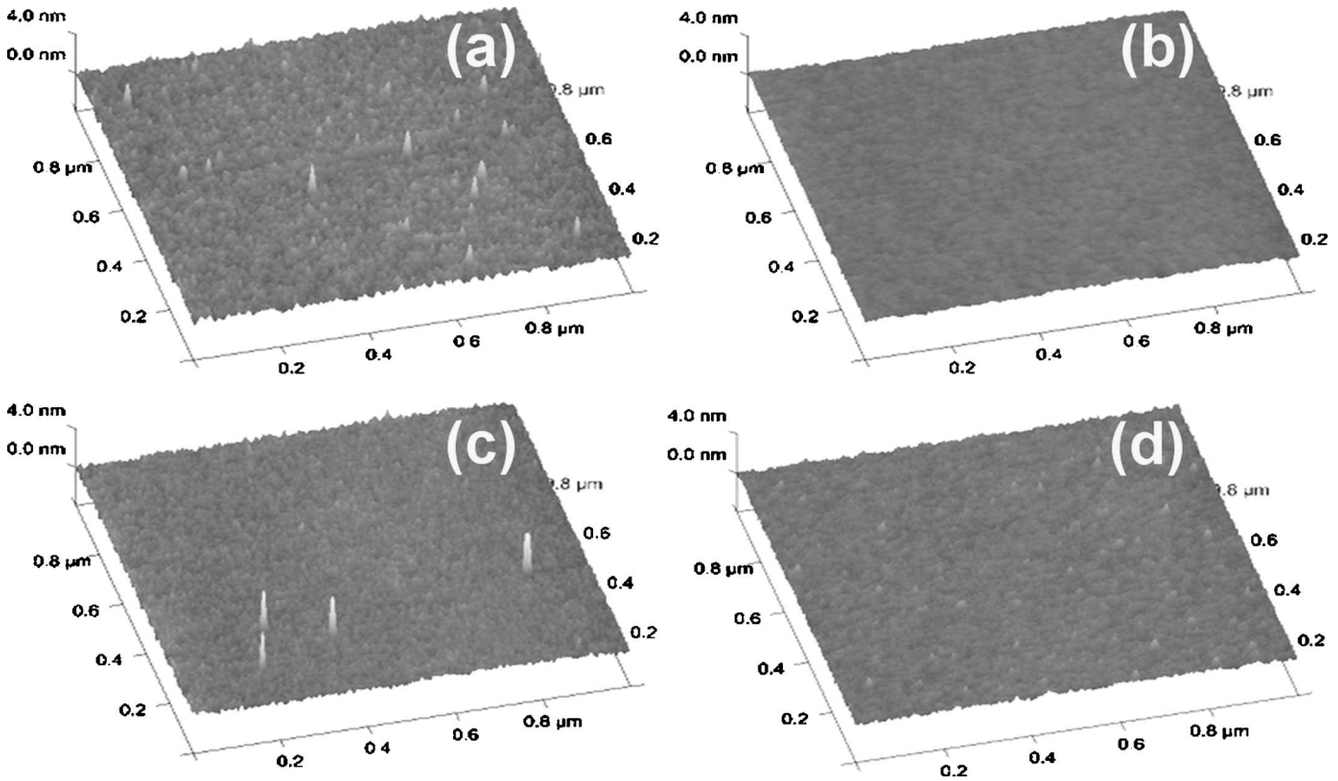

Figure 1. AFM images of 4 nm CeO_2–HfO_2 laminates on silicon, deposited at different temperatures from 220 to 520 °C. (1 × 1 µm images, depth scale is 4 nm). (a) 220 °C, (b) 320 °C, (c) 420°C, (d) 520°C.

with presence of interlayer diffusion and reactions that can take place in the dielectric.[5-9] In this work, two different methods for extracting the electrical properties of the laminates were used: (*i*) CVC simulation by Hauser, which includes quantum-mechanical effects and gate depletion[10] and (*ii*) a technique proposed by Kar for dielectric capacitance extraction.[6] Comparison of the results achieved by the two methods is found to be useful for preventing the major errors in equivalent oxide thickness (EOT) extraction.

C-V and current-voltage (*I-V*) measurements of layers were performed at a probe station using an HP4275A analyzer and HP4140B pA-meter at room temperature and at 10 kHz, 100 kHz, and 1 MHz frequencies. Conductance data from 10 kHz measurement is used for calculating density of interface states.[11] A dual frequency-correction method[5] was used to extract the series-resistance-corrected capacitance by using 100 kHz and 1 MHz measurement data. Dual frequency-corrected capacitance values were then processed in two different models to extract the electrical properties of the layers, i.e., EOT and the flatband voltage (V_{FB}).

Figure 4 shows the double frequency-corrected *C-V* data of the laminated layers with different thicknesses from 2 to 8 nm, depos-

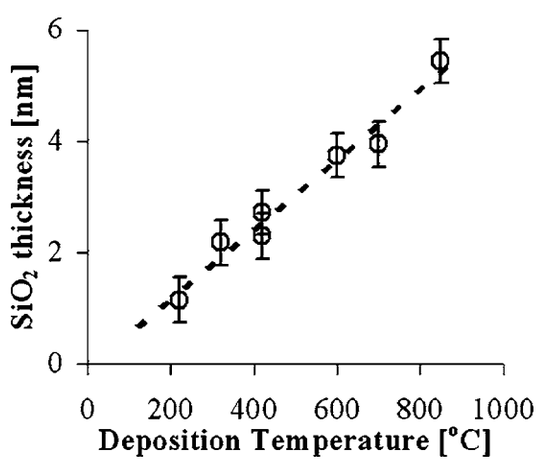

Figure 2. Dependence of interface SiO_2 thickness, measured by XPS, on deposition temperature.

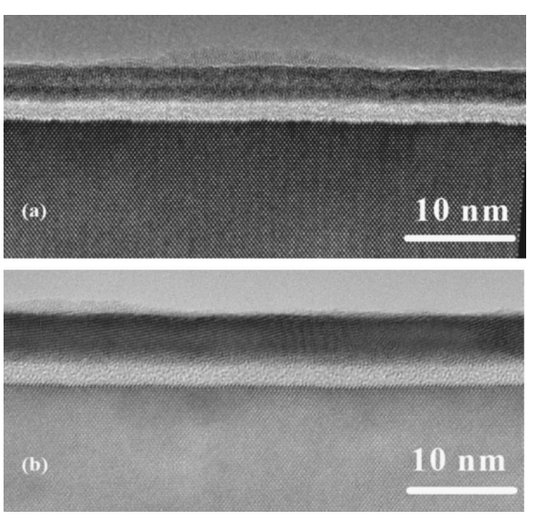

Figure 3. Cross-sectional TEM image of laminated layers (a) deposited at 420 °C, (b) deposited at 520 °C (both image width is 50 nm).

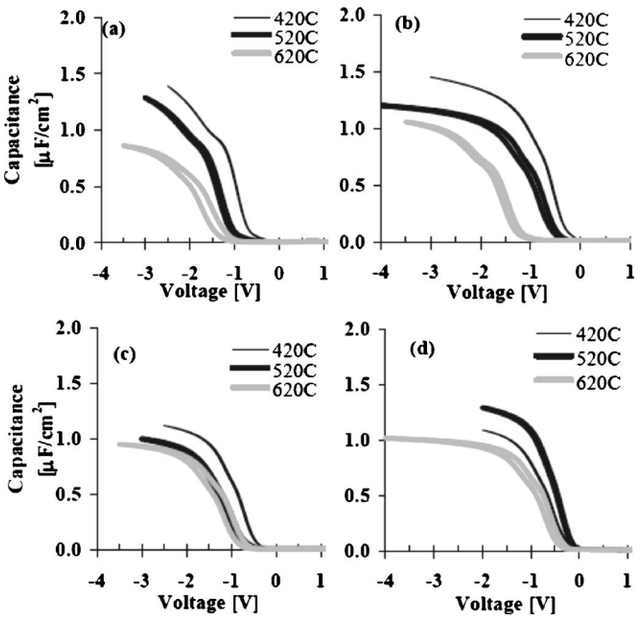

Figure 4. Dual frequency-corrected *C-V* curves of CeO_2–HfO_2 laminates at different thicknesses deposited at different temperatures. (a) 2 nm layers, (b) 4 nm layers, (c) 6 nm layers, (d) 8 nm layers.

ited at various temperatures. All figures refer to as-deposited (including in situ PDA) layers, with no forming gas anneal (FGA) applied after metallization. *C-V* plots showed higher hysteresis for increasing deposition temperature and very low (less than 40 mV) hysteresis for the layers deposited at 420°C, till 2.5 V in accumulation. This indicates an increased charge density in the layers at elevated deposition temperatures, which correlates to the increased crystallinity. However, the difference of the accumulation voltages also affects the *C-V* hysteresis: For the layers deposited at higher temperatures, with higher V_{FB} than the ones deposited at lower temperatures, higher accumulation voltages in *C-V* measurements were used. Figure 5a shows the extracted EOT values of the layers deposited at different temperatures and thicknesses. Corresponding leakage current densities are presented in Fig. 5b.

Using the SiO_2 thicknesses measured by XPS for different layer thicknesses deposited at 420°C, the dependence of dielectric constant of laminates on layer thickness is calculated by using a simple, series-connected two parallel plate capacitor model. Here, the dielectric constant of the interfacial oxide is assumed to be equal to that of SiO_2 for all thicknesses and plotted as such in Fig. 6a. As shown in the figure, the *k* value of the laminates is in levels of 5 for the thin deposited layers. This result can be explained by the increase of the *k* value of the IL by mixing of the SiO_2 with CeO_2,

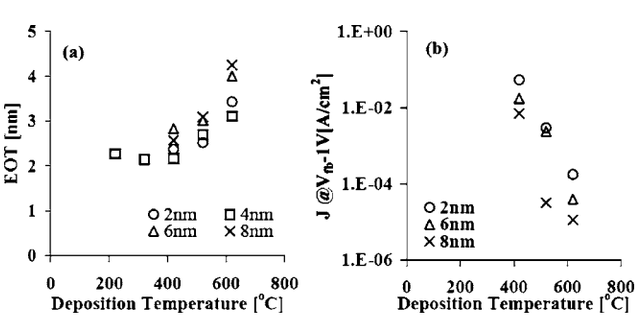

Figure 5. (a) Equivalent oxide thickness and (b) leakage current density of different thickness CeO_2–HfO_2 laminates deposited at various temperatures.

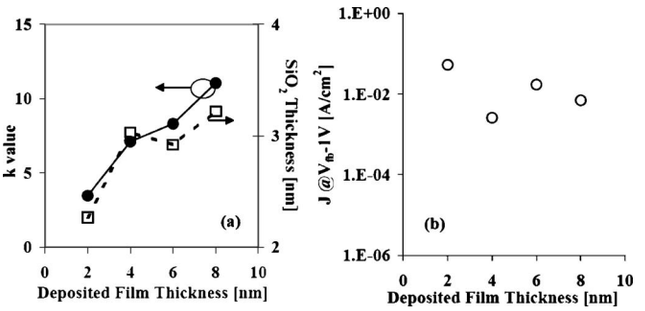

Figure 6. (a) Calculated dielectric constant of layers deposited at 420°C and (b) corresponding leakage current densities (*J*) of layers at 1 V beyond V_{FB}.

which is the first layer of the laminate. Because the *k* value of such a mixed oxide layer is expected to be higher than 3.9, the calculations result in lower *k* values for the laminated layer. However, the effect of the IL on the whole stack decreases by the increasing deposited layer thickness. The dependence of the *k* value on deposited layer thickness for thicker layers chiefly depends on the increased crystallinity in thicker layers. The leakage current density (*J*) at 1 V beyond V_{FB} of the same layers, which is shown in Fig. 6b, also confirms such explanation: The layers with 6 and 8 nm thicknesses have higher leakage current density compared to the thinner ones. This correlates to the increased leakage through grain boundaries in the polycrystalline structure. Increased crystallinity of the thicker layers also agrees with the increased *k* values.

In Fig. 7, the electrical properties of layers deposited at 520°C under reducing and oxidizing ambient are compared. EOT-deposited layer thickness plots are presented in Fig. 7a and c. According to the linear fits of EOT-deposited layer thickness plots, layers deposited in reducing ambient have a *k* value around 30, whereas the ones deposited in oxygen are around 15. However, the layers deposited in oxygen ambient have lower interface oxide EOT of approximately 0.8 nm, whereas the ones deposited in reducing ambient have around 1.9 nm. This can be the result of decreased effect of the in situ PDA on the layers deposited in oxygen ambient, where the

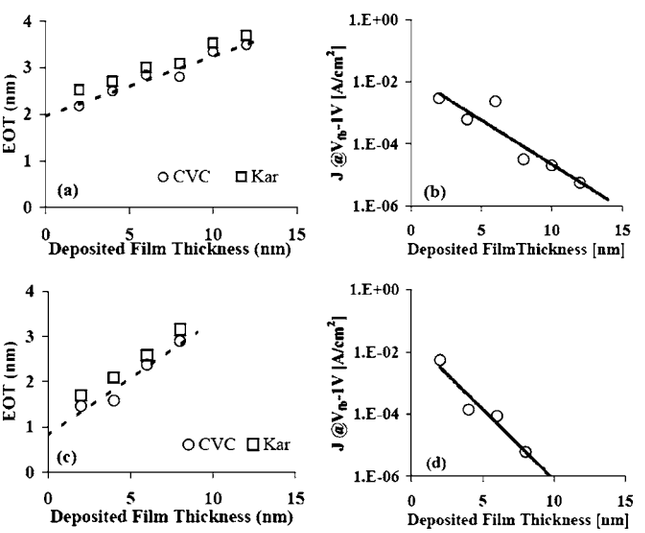

Figure 7. Extracted EOT and leakage current density at 1 V beyond V_{FB} of layers deposited at 520°C at reducing atmosphere ($Ar + H_2$) compared with the ones deposited at same temperature at oxygen backpressure. (a) EOT of the layers deposited at $Ar + H_2$. (b) Leakage current density of the layers deposited at $Ar + H_2$. (c) EOT of the layers deposited at O_2. (d) Leakage current density of the layers deposited at O_2.

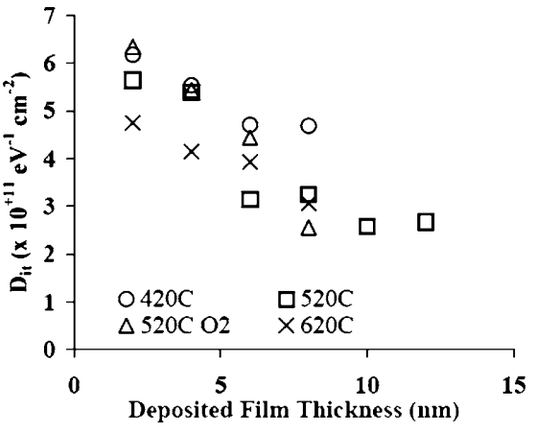

Figure 8. Density of interface states of CeO_2–HfO_2 laminates deposited at different temperatures. D_{it} values of oxygen deposited layers are also shown in the figure (520°C O_2).

layers are already oxidized during deposition and interface oxide is more stabilized during deposition. As a result of higher interfacial oxide stability in oxygen ambient deposition, interface oxide thickness is found to be less than the ones deposited at reducing ambient. Another reason of this effect can be the interface oxide alloying with CeO_2 first layer, which results in lower EOT for interface oxide. However, this difference also agrees with the thickness dependency of the layers deposited in reducing ambient: As explained previously, thinner layers are more transparent to oxygen diffusion during PDA and this increases the EOT of the thinner layers. Additionally, thicker layers have higher crystallinity, which decreases the EOT of the layers. Therefore, the slope of the linear fit in EOT-deposited layer thickness plot is suppressed by the combination of these two factors and may lead to erroneous k value calculation.

The effect of layer thickness on the interface properties can be seen more clearly by comparing the density of interface states (D_{it}) of layers deposited at different temperatures and ambient, followed by in situ PDA (Fig. 8). D_{it} values have a tendency to stabilize for thicker layers, where the effective oxygen diffusion to interface during in situ PDA is limited comparing the thinner ones. D_{it} values for all layers are in the order of 10^{11} cm^{-2} levels and tend to decrease with increasing deposition temperature and for increasing layer thickness.

Conclusions

The physical and electrical properties of CeO_2–HfO_2 nanolaminates deposited by PLD on Si(100) were investigated. It was shown that when layers were deposited in a reducing ambient and oxidized by in situ PDA, their properties depend strongly on their layer thickness. For 420°C deposited layers, lower thicknesses', approximate k values are of the level of 8, where the thicker ones reach up to 15. This difference correlates to the increased crystallinity of the layers with increasing physical thickness.

The highest k value of 30 is found for the layers deposited at 520°C in reducing ambient where the ones deposited in oxygen have a lower k value of 15. The lowest EOT of 1.5 nm is found for 2 nm physical thickness layer deposited at oxygen ambient at 520°C, and the highest EOT for the same physical thickness belonging to the layer deposited at 620°C is 3.1 nm. Leakage current densities of these layers are 5.5×10^{-3} and 1.8×10^{-4} A cm^{-2}, respectively. The lowest leakage current of 5.6×10^{-6} A cm^{-2} is found for 12 nm physical thickness layer deposited at 520°C in reducing ambient; however, the 8 nm physical thickness layer deposited at oxygen ambient at same temperature is 6.1×10^{-6} A cm^{-2}, which is significantly better than the other layer with 8 nm physical thickness.

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