Title: Scalable Correlator Architecture for Energy-efficient Radio Astronomy Processing

Approximate computing allows controlled errors to increase computing efficiency. An increase in computing efficiency means a reduction in computing costs like power/energy consumption. However, the introduction of errors reduces the precision of computing and/or compromises the output quality. Therefore, the design target in approximate computing is to achieve the best efficiency design while providing a sufficient quality of output.
In our recent study, we have analyzed a simple correlator model for radio astronomy processing. Our analysis approves the feasibility of approximate multipliers for energy-efficient correlator processing. This assignment focuses on implementing the model and researching promising approximate multiplication techniques to design a scalable and energy-efficient correlator architecture.
The assignment includes the following steps:

1. Understanding the correlator model and perform analysis to indicate dominant (power-hungry) components
2. Implementing the model on FPGA (and/or ASIC) to perform hardware cost analysis (chip-area, power consumption, latency)
3. Researching approximate multiplier techniques promising for the correlator design
4. Optimizing the correlator architecture for minimum power/energy consumption, which satisfies the output quality criterion of radio astronomy processing.

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