SparkRV: Open Source Many-Core Digital Neuromorphic Processor

Sameed Sohail, Mattias Westerink, Wiebren Wijnstra, Sharon Moolenaar, Berend-Jan van der Zwaag, Sabih Gerez, Amirreza Yousefzadeh

SparkRV (work in progress) is an open-source, many-core digital neuromorphic processor built on the flexible RISC-V architecture, specifically optimized for **low-power, embedded AI applications**. Featuring a

- Data-centric
- Near-memory
- Event-driven
- Dataflow

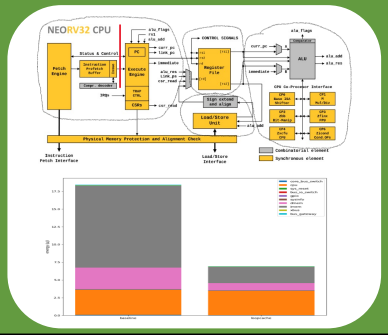
design. SparkRV efficiently handles low-power real-time inference and on-device learning tasks by working in event-driven mode. Each independent core integrates a NeoRV RISC-V processor, dedicated data memory, and a specialized accelerator seamlessly interconnected via a scalable network-on-chip (NoC) architecture. Designed to scale effortlessly through chiplet integration, SparkRV facilitates efficient communication among cores using small data packets, enabling powerful yet energy-efficient neuromorphic computing solutions.

ULP RISC-V

Reducing the power consumption of RISC-V through the instruction loop cache

Wiebren Wijnstra

- Standard cell-based tiny loop cache
- Both dynamic and static caching mechanisms

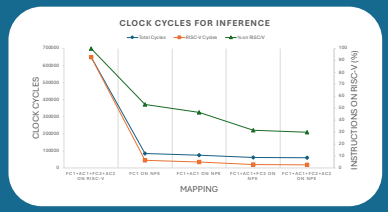


Digital SNN Accelerators

Programmable co-processor for low-precision inference of AI applications

Mattias Westerink

- Tightly-coupled with memory
- Low-precision arithmetic
- Dedicated loop-buffer to exploit the highly recurrent patterns present in neural networks
- Exploit sparsity in weights and activations

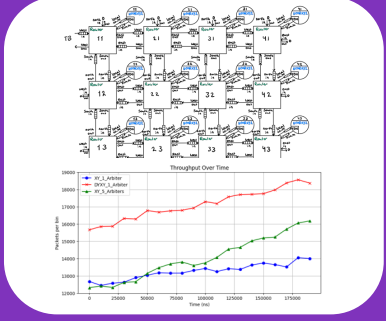


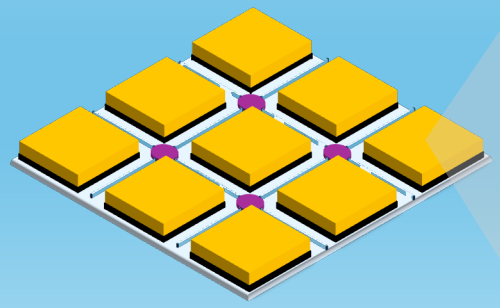
NoC

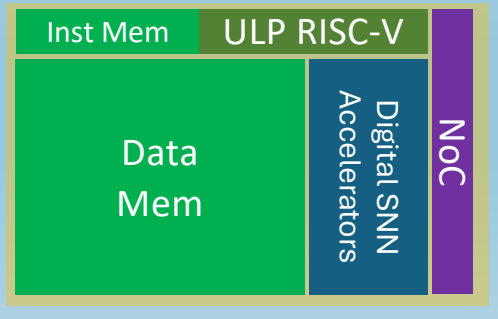
Scalable Network on Chip with low area footprint

Sharon Moolenaar

- Ultra-low overhead
- Dynamic X-Y routing
- Designed for tiny packets of data







Target technology: Global Foundries FDX 22nm
Simulation and verification with Cadence Xcelium (RTL simulation), Genus (area measurement, timing) and Joules (power measurement)

Computer Architecture for Embedded Systems (CAES)

Please contact us if you want to know more

a.yousefzadeh@utwente.nl