Thesis Topic: Aging-Aware Run-Time Management and Scheduling

Background

As embedded systems continue to evolve with smaller and faster technologies, **hardware aging** becomes a critical challenge [2] —especially in **safety-critical applications** such as aerospace, automotive, and space systems. Over time, physical effects like **Negative Bias Temperature Instability (NBTI)**, **Time-Dependent Dielectric Breakdown (TDDB)**, and **Hot Carrier Injection (HCI)** degrade the performance of transistors, potentially leading to **incorrect or delayed operations** [1], when the critical paths become longer than the clock cycle time. Moreover, different workloads lead to a different amount of stress so that joint consideration of timing effect and the aging issue is thus needed [3].

Traditional real-time system designs often neglect aging effects, risking the validity of **Worst-Case Execution Time (WCET)** estimates and system safety. A large majority of existing real-time approaches focuses on typical hardware faults [4], such as soft errors and permanent faults. Few relevant approaches exist, and they deal with aging focusing in memories, e.g., considering HCI and BTI for L1 caches [5], and register files [6]. As a result, novel approaches are required to deal with electronic aging in modern technologies and its impact on timing guarantees.

Thesis Objective

This thesis aims to **develop aging-aware runtime strategies** that adapt to hardware degradation over time—without compromising **real-time guarantees**.

You will:

- Analyze how aging affects WCET and scheduling decisions
- Propose **safe runtime control mechanisms** for **self-healing and dynamic scheduling**
- Develop techniques to adapt **WCET estimations, hardware configurations**, and **task scheduling** to mitigate aging impact

Moreover, you may have a chance to shortly stay to visit research institutes in France to closely work with more international researchers.

Tools & Platforms

- **Open-source processors** (e.g., RISC-V)
- **Real-time operating systems** (e.g., FreeRTOS)
- WCET analysis and scheduling tools
- Simulation or emulation platforms to model aging and execution timing

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Learning Outcomes

- Understanding of **electronic aging phenomena** in modern technology nodes
- Familiarity with **real-time systems**, **scheduling theory**, and **runtime system design**
- Experience in **embedded systems development**, **hardware-software co-design**, and **reliability analysis**

Key References:

[1] N. Landeros Muñoz, A. Valero, R. Gran Tejero, and D. Zoni. Gated-cnn: Combating nbti and hci aging effects in on-chip activation memories of convolutional neural network accelerators. Journal of Systems Architecture, 128:102553, 2022

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[3] S. Rehman et al., "Cross-Layer Software Dependability on Unreliable Hardware," in IEEE Transactions on Computers, vol. 65, no. 1, pp. 80-94, 1 Jan. 2016, doi: 10.1109/TC.2015.2417554

[4] C. Maiza, H. Rihani, J. Rivas, J. Goossens, S. Altmeyer, and R. Davis. A Survey of Timing Verification Techniques for Multi-Core Real-Time Systems. ACM Computing Surveys (CS), 52(3):56:1–56:38, June 2019

[5] D. Trilla, C. Hernandez, J. Abella, and F.J. Cazorla. Aging assessment and design enhancement of randomized cache memories. Trans. Device and Materials Reliability (TDMR), 17(1):32–41, 2017.

[6] I. Tuzov, P. Andreu, L. Medina, T. Picornell, A. Robles, P. Lopez, J. Flich, and C. Hernández. Improving the robustness of redundant execution with register file randomization. In Int. Conf. Computer Aided Design (ICCAD), page 1–9. IEEE Press, 2021

Interested?

If you're passionate about **reliability**, **embedded systems**, and making a **real impact** in future safety-critical applications, send us an email, write a bit about your motivation to work on the subject, your background, and at what stage of the master program you are. We will then set a meeting.

- Supervisor: Dr.-Ing. Kuan-Hsun Chen, Email: k.h.chen@utwente.nl
- External Supervisor: Prof. Angeliki Kritikakou, Email: angeliki.kritikakou@irisa.fr