Thesis Topic:

Lightweight Error Handling Schemes for Biased Error Models in Emerging Technologies

Background:

In this era, where the large scale of data is rapidly generated and stored in computer systems, existing memory and storage media have confronted serious challenges, such as "memory wall", to fulfill the demands of various advanced applications. To overcome these shortcomings, emerging memory technolgoies, such as spin-torque transfer random-access memory (STT-RAM), resistive random-access memory (ReRAM), phase-change memory (PCM) and racetrack memory (RM), gradually become promising solutions due to their ideal access performance, energy efficiency, storage capacity, and non-volatility.

Racetrack memory (RM) features high integration density, low unit cost and low energy consumption [1], which have been considered as scratchpad memories intergrated in the computer systems. However, in RMs, data cannot be randomly accessed. The track needs to be shifted to let the data align with an access port first before it can be read out. The distance, i.e., how far the track needs to be shifted, defines the additional shift latency. While researches have been working on the reduction of shifts to improve the runtime efficiency, RM also exhibits unique reliability issues, such as the position error and data representation problem [2]. Novel error detection and correction schemes have been proposed for Domain-Wall RM, albeit with added performance and energy overheads. However, the reliability concerns of skyrmion RM have garnered little attention [3]. Developing lighweight error handling schemes is highly relevant to push forwward the applicability of RM in the real world systems.

Project Description:

This project aims to develop error handling schemes, which is able to detect and correct the error induced by the inherent shift mechanism, that takes into account the tradeoff between the overhead and the effectiveness. The student is expected to analyze the state-of-the-arts and develop a new methodology taking into account, e.g., the biased error models imposed by Skyrmion RM, while minimizing the shift latency. The student will then evaluate the overhead of the proposed error handling schemes in the trace-based simulator, namely RTSim, and the performance impact incurred by the proposed method.

Key References:

1. A Comparative Cross-layer Study on Racetrack Memories: Domain Wall vs Skyrmion
2. Hi-fi playback: tolerating position errors in shift operations of racetrack memory
3. Granularity-Driven Management for Reliable and Efficient Skyrmion Racetrack Memories
4. RTSim: A Cycle-accurate Simulator for Racetrack Memories

Student Profile:

Skills Required:

- Proficiency in C programming

Desired Knowledge:

- Advanced Computer Architecture
- Dependable Computing

Supervisor/Contact Information:

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How to Apply:

Send us an e-mail to k.h.chen@utwente.nl and m.ottavi@utwente.nl, write a bit about your motivation to work on the subject, your background, and at what stage of the master program you are. We will then set a meeting.
