MSc Thesis - Fault Injection Campaign

Thesis Topic:

Fault Injection Simulation Campaigns on Hardware RTL layer

Background:

Hardware RTL (Register-Transfer Level) is a high-level abstraction for digital design, commonly used in the design of ASICs and FPGAs. RTL describes how data flows between registers and how the logical functions between them operate on the data. It's often written in hardware description languages like VHDL or Verilog. RTL allows for timing analysis, functional verification, and is synthesizable into gate-level descriptions. It serves as a critical step in the hardware design flow, bridging the gap between high-level architecture and low-level gate-level design.

RTL fault injection campaigns are methods used to assess the dependability and fault tolerance of a hardware system at the RTL design phase. These campaigns involve deliberately introducing faults, such as bit-flips or stuck-at faults, into the RTL code using hardware description languages like VHDL or Verilog. The primary goal is to simulate how the hardware behaves under erroneous conditions, which is crucial for safety-critical or mission-critical applications. These campaigns help designers identify weaknesses in the system early in the development cycle, allowing for improvements before moving on to more expensive stages like gate-level synthesis or physical fabrication.

Project Description:

The project aims to execute a robust, statistically-grounded fault injection campaign, leveraging the vRTLmod tool to target RISC-V core architectures. Originating from the Technical University of Munich, this cutting-edge simulator is built upon the Verilator framework and coded in C++.

Both the simulator code and the core's HDL are already available. The main work will involve integrating these two elements, exploring statistical methods tailored for fault injection, and comprehensive result analysis and presentation.

The student will explore and identify RISC-V processor components vulnerable to faults, with the possibility to suggest and test modifications. Given the project's intersection with areas of interest to our external collaborators—namely the European Space Agency, NLR (Nederlands Lucht- en Ruimtevaartcentrum), and various industry stakeholders—students will have the unique opportunity to synergize with projects directly impacting these organizations.

Key References:

1. vRTLmod: An LLVM based Open-source Tool to Enable Fault Injection in Verilator RTL Simulations
2. vrtlmod github
3. The NEORV32 RISC-V Processor github
4. Statistical fault injection: Quantified error and confidence

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Student Profile:

Skills Required:

- Proficiency in C/C++ programming
- Knowledge about HDL
- Willingness to dive into statistics

Previous Knowledge:

- ECA 1
- Digital Design
- Dependable Computing Systems (is a plus, but not a requirement)

Supervisor/Contact Information:

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How to Apply:

Send us an e-mail to m.ottavi@utwente.nl and b.endresforlin@utwente.nl, write a bit about your motivation to work on the subject, your background, and at what stage of the master program you are. We will then set a meeting.
