Exploring RISC-V Customized Extensions for Technology-Agnostic Computing in Memory

With the rapid advancements in AI and ML, enabling memory to perform computations has become increasingly crucial in eliminating the data movement bottleneck that plagues current system designs. To provide application developers with a convenient programming environment akin to CUDA, researchers have been diligently investigating suitable programming models and potential compilation optimizations for automating software mapping on such emerging memory architectures.

In this thesis, we propose an in-depth exploration and development of customized extensions for the RISC-V instruction set architecture. By surpassing the limitations of conventional instructions, these extensions aim to empower applications to seamlessly leverage a diverse range of memory technologies in the future and open a door to further optimize the automation via compilation techniques.

Join us on this exciting research journey, where you will have the opportunity to make significant contributions to the field and pave the way for future advancements in computing.

Project Objectives:

- Comprehensive Study: Conduct an in-depth review of existing computing in-memory architectures, exploring their strengths, weaknesses, and potential pitfalls in achieving technology-agnostic computing.
- RISC-V Architecture: Acquire a solid understanding of the RISC-V instruction set architecture and its extensibility features, including the privileged specification and memory management capabilities.
- Customized Extension Design: Devise innovative approaches to design customized RISC-V extensions that can efficiently handle diverse technologies in memory, such as heterogeneous memory systems, non-volatile memory, and specialized accelerators.
- Performance Evaluation: Implement the customized extensions and evaluate their impact on system performance, including metrics like memory bandwidth, latency, power consumption, and scalability.

If you are interested in this project and would like to learn more, please feel free to contact our research supervisors, Kuan-Hsun Chen (k.h.chen@utwente.nl) and Marco Ottavi (m.ottavi@utwente.nl).