# On-chip scan pattern retargeting

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**Keywords**: IEEE 1687, IJTAG, Retargeting, Scan.

**This thesis requires knowledge of:** Digital design and VHDL, FPGA design flow, behavioural and post-synthesis simulations using QuestaSim.

## Description:

Silicon technology scaling and the increasing reliance on design reuse and automation lead to very complex System-on-Chips (SoCs). Testing and debugging of such complex SoCs is a challenging task. Consequently, dedicated IPs for testing and debugging, referred to as Embedded Instruments (EIs), have been increasingly integrated into SoCs. For instance, temperature sensors, voltage monitors, current sensors, Built-In-Self-Test engines and many others.

With the increased integration of heterogeneous EIs, a need emerged for standardizing their access methods. In 2014, the IEEE 1687 standard (also known as IJTAG) was ratified, in order to provide standardized access and operation methods for the EIs. The IEEE 1687 standard introduces a flexible EI network based on reconfigurable scan chains such networks are often called IJTAG networks or Reconfigurable Scan Networks (RSNs). The standard follows a descriptive approach rather than a prescriptive one for defining the construction of the network. Hence, a very large design space of IEEE 1687-compliant networks becomes possible. Figure 1 shows an example of an RSN, other examples are shown by the set of IEEE 1687 benchmark networks [1].

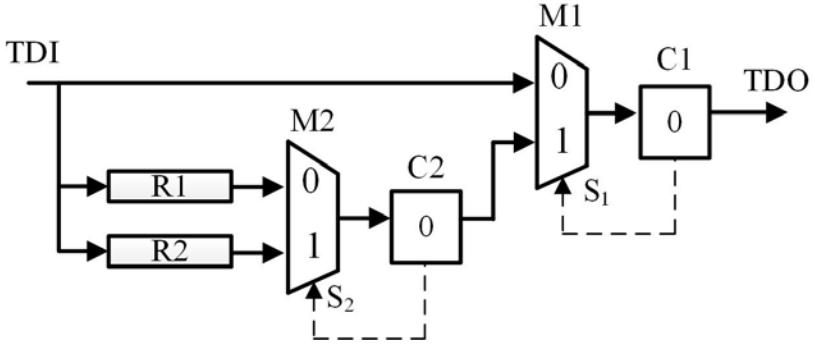


*Figure 1. An RSN with two instrument ScanRegisters (R) and two network configuration ScanRegisters (C) and two ScanMuxs (M).*

Pattern retargeting is the process of translating an instrument-level pattern into several network-level scan vectors [2]. Pattern retargeting can become a complex procedure with the increased complexity of the networks. A novel light-weight methodology, referred to as structured retargeting, has been presented in [3]. Structured retargeting is an efficient methodology for performing dynamic (run-time) retargeting.

**The goal of this MSc. thesis** is to evaluate the performance of two different on-chip variants of structured retargeting [4]. First the student should design a micro-architecture for each structured retargeting variant as standalone accelerators. Both designs should be implemented in RTL (VHDL) with a focus on minimizing the retargeting time and the area overhead. Different design trade-offs of the micro-architecture should be studied, evaluated and reported. The student is expected to extensively verify both designs against a set of benchmark circuits [1] and against other challenging networks that will be provided.

The student will quantitatively evaluate the performance of both on-chip structured retargeting variants using the developed designs, and report any performance bottlenecks. Subsequently, the student will investigate and evaluate any necessary modifications to the original on-chip structured retargeting methods as reported in [4]. An FPGA (using Xilinx VC707 evaluation board) implementation will be carried out and verified, also the design will be synthesized for ASIC (TSMC 40nm) and verified using post-synthesis simulations.

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**References:**

[1] http://fp7-bastion.eu/index.php?page=30

[2] F. Ghani Zadegan, U. Ingelsson, E. Larsson and G. Carlsson, "Reusing and Retargeting On-Chip Instrument Access Procedures in IEEE P1687," in *IEEE Design & Test of Computers*, vol. 29, no. 2, pp. 79-88, April 2012.

[3] A. Ibrahim and H. G. Kerkhoff, "Structured scan patterns retargeting for dynamic instruments access," *2017 IEEE 35th VLSI Test Symposium (VTS)*, Las Vegas, NV, 2017, pp. 1-6.

[4] A. Ibrahim, “Test standards reuse for structured and cost-efficient dependability management of system-on-chips,” Ph.D. thesis, university of Twente, 2018.