Boost FPGA Performance by using High Clock Frequencies

The utilization of the used FPGA resources in time is rather low compared to an ASIC due to the lower clock frequency. The efficiency of FPGA resources (lookup tables) can be increased by using designs with many pipeline stages combined with a very high clock frequency. However, designs with clock frequencies up to 500 MHz needs sophisticated placement and routing techniques to hold the timing constraints.

In this work, the automatic insertion of pipeline stages in data paths after synthesis and the usage of high clock frequencies should be investigated. The overall goal is to increase the efficiency and performance of FPGAs. The data paths of critical parts of a design should be analyzed and additional pipeline stages should be automatic inserted. Moreover, the placement and routing of these pipeline stages should be investigated in order to reach a high clock frequency.

Prerequisites:	Good knowledge in FPGA design
Type of Work:	Theory (30%), Conception (40%), Implementation (30%)
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