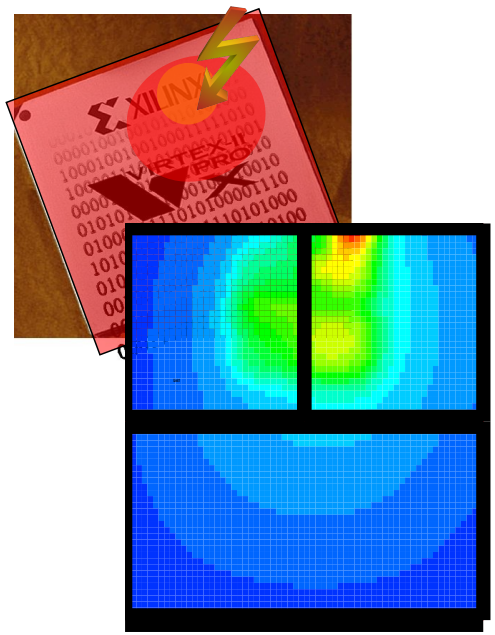
Increasing FPGA Lifetime by Dynamic Reconfiguration

Ever shrinking device structures allow on the one hand the implementation of more complex systems, whereas, on the other hand, this trend results in an increased susceptibility to radiation and temperature-dependent aging effects. This holds also true for future FPGA devices which suffer from the heat produced from computationally-intensive modules. These modules may therefore accelerate FPGA aging locally. Now, dynamic reconfiguration may help to distribute highly-active modules in a way that the wear is equalized over the FPGA area. By using such techniques, the lifetime of the FPGA can be increased significantly.



In this thesis, the local FPGA temperature dissipation should be estimated at run-time and modeled with the help of expected activities of modules. Such temperature information can be used by an available method to determine a better module placement with respect to FPGA aging.

Prerequisites:	Good knowledge in software programming (e.g., Java or C++)
Type of Work:	Theory (30%), Conception (40%), Implementation (30%)
Supervisor:	Daniel Ziener (d.m.ziener@utwente.nl)