# Embedded Instrument Networks

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**Keywords**: IEEE 1687, IJTAG, Embedded Instruments.
**This thesis requires knowledge of:** Digital design and VHDL, behavioural simulations using QuestaSim, MATLAB.

## Description:

Several non-functional components are being integrated in modern System-on-Chips in order to monitor the physical/logic state of the system and to perform dynamic adaptation of the processing environment, collectively referred to as Embedded Instruments (EIs). For instance, workload monitors, fault detectors and clock gating circuits. Several previous works have introduced dedicated networks for accessing EIs, which includes optimized buses and Network-on-Chips (NoCs). With the introduction of the IEEE 1687 standard (IJTAG) a flexible access network to EIs can be designed. Multi-mode IJTAG networks provides an architectural extension of the IEEE 1687-defined networks to enable efficient interrupts delivery and localization [1].

**The goal of this MSc. assignment** is to evaluate the efficiency of multi-mode IJTAG networks as an EI network compared to state-of-the-art ones, and identify any limitations. The student will start with performing literature review on the available EI networks, and selects a set of networks for evaluation based on reasonable criteria. Subsequently, a quantitative evaluation of the performance (in terms of latency and bandwidth) and overhead (area and power consumption) of the selected networks along with multimode-IJTAG networks will be performed. The scalability of EI networks is an important factor of such evaluation.

***Successful completion of this thesis could lead to a joint publication.***

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## References:

[1] A. Ibrahim and H. G. Kerkhoff, “Efficient utilization of hierarchical iJTAG networks for interrupts management". In 2016 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT), pp. 97-102, Sept 2016.